The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC851

Multifunction I/O

(16 bit ADC/DAC, TTL I/O, Counter)

Version 2.2

User Manual

Issue 2.2.0

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TPMC851-10R

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(16 bit ADC/DAC, TTL I/O, Counter)

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	Initial Issue	May 2004
1.1	Added ADC power-up note	January 2005
1.2	Correction Interrupt Control Register ICR, Summarization of Important Notes	February 2006
1.3	New address TEWS LLC	September 2006
1.4	Changed PCI9030 Local Configuration Clarified Sequencer Start / Stop Control in ADCSEQCONT	September 2006
1.5	Added note to ADC Control Register	October 2006
1.0.6	New notation for HW Engineering Documentation Releases	March 2009
1.0.7	Corrected DAC Data Register Reset Value to 0x0000	January 2010
1.0.8	General Revision	August 2014
1.0.9	"PCI Base Address 2 for Local Address Space 0" initial value corrected in Table "PCI9030 Header"	September 2014
2.0.0	User Manual Update for TPMC851 V2.0.	September 2022
2.1.0	User Manual Update for TPMC851 V2.1.	May 2024
2.2.0	Added new register “ADC Settling Time Register ADCSETTLING”	January 2025

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1 Product Description

The TPMC851 combines 32 single ended / 16 differential channels of 16 bit multiplexed analog input, 8 channels of 16 bit analog output, 16 digital I/O lines and 2 32 bit multi-purpose counters on a standard single-width PMC module.

A 16 bit ADC converts 32 single-ended or 16 differential multiplexed ADC input channels. The data acquisition and conversion time is up to 1.25µs without channel/gain change and up to 17.25µs with channel/gain change (ADC throughput rate up to 250ksps). The input multiplexer of the A/D circuit offers analog overvoltage protection of up to 70Vpp. A programmable gain amplifier allows gains of 1, 2, 4 or 8 resulting in input voltage ranges of ±10V, ±5V, ±2.5V or ±1.25V.

The ADC part of the TPMC851 can operate in Manual Mode or Sequencer Mode:

- Manual Mode

  In Manual Mode the multiplexer, programmable gain amplifier and the converter are fully controlled by the user. A conversion for a selected channel / gain can be started automatically after the settling time has elapsed, or manually by the user.

- Sequencer Mode

  In Sequencer Mode each of the A/D channels can be independently enabled and configured for the sequencer. The sequencer can run continuously, at specific time intervals, or it may be triggered by an external event. Conversion data is buffered in a data RAM.

The 8 analog output channels are utilized by eight 16 bit digital to analog converters (DACs). The conversion time is 10 µs. An operational amplifier drives the full-scale range of ±10V and is capable to drive high capacitive loads. Similar to the analog inputs a sequencer can control the analog outputs. Following operation modes are available:

- Immediate Update: Updates the DAC output immediately when new data is written to the DAC channel.
- Simultaneous Update: DAC data is buffered and all DAC outputs are updated simultaneously on a trigger event:
  - Manual Update: Updates all DAC outputs on a manual event (register write)
  - Trigger Update: Updates all DAC outputs on an external event
  - Sequencer Update: Updates all DAC outputs after the sequencer timer has elapsed

For each individual TPMC851 card, A/D and D/A correction values are obtained during the factory acceptance test and are stored in an on-board EEPROM.

The 16 digital TTL tri-state I/O lines with 4.7kΩ pull up resistors are ESD protected. All 16 lines can be individually programmed as input or output, and can generate an interrupt on negative and positive transitions. Each input has an electronic debounce circuit to prevent short spikes on the input lines to cause an interrupt. The digital inputs can supply the external signals for the ADC and DAC sequencer and the 32 bit counters.

The TPMC851 offers 2x 32 bit multi-purpose counters. Each counter includes a 32 bit preload register and a 32 bit compare register. The 32 bit counters can be fed with an internal clock or with an external signal supplied by the digital inputs. The 4 counter input modes determine the interpretation of the input signals. Additionally, 3 count modes, which describe the behavior of the counters, and 4 control modes are available.

- Counter input modes:
  - Internal clock with prescaler
  - Up/Down count: first counter input counts up, second input counts down
  - Direction count: first counter input counts, second input sets count direction
  - Quadrature count with 1x, 2x or 4x resolution multiplier
- Count modes:
  - Cycling Counter: normal wrap-around count mode
  - Divide-by-N: counter is reloaded from the preload register upon a borrow or carry
  - Single Cycle: counter stops upon a borrow or carry
- Control Modes:
  - Load on Control: counter is reloaded from the preload register
  - Latch on Control: counter value is latched
  - Gate on Control: counter input is gated
  - Reset on Control: counter is reset

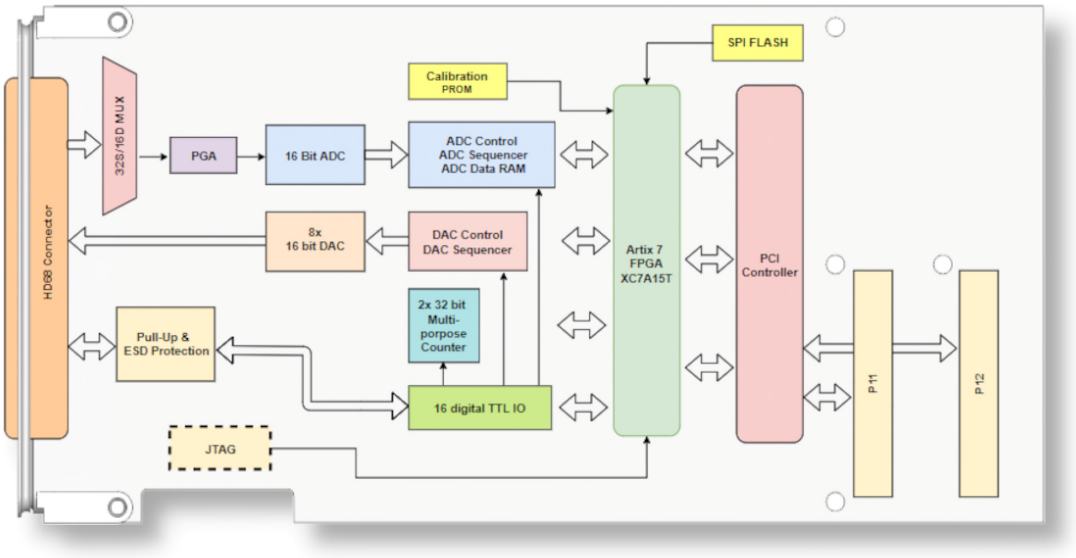

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface	
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size
Electrical Interface	PCI Rev. 3.0 compatible 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage
On Board Devices	
PCI Target Chip	TEWS PCI Interface FPGA
ADC	AD7663
DAC	DAC7644
Analog Input	
Number of Analog Inputs	32 single-ended or 16 differential channels
Input Gain Amplifier	Programmable for gain 1, 2, 4 and 8
Input Voltage Range	±10V for gain = 1 ±5V for gain = 2 ±2.5V for gain = 4 ±1.25V for gain = 8
Input Overvoltage Protection	70Vpp
Correction Data	A/D Correction data for gain and offset stored in EEPROM
Resolution	16 bit with no missing codes
Conversion Time	1.25µs without channel/gain change (ADC throughput rate up to 250ksps) 17.25µs with channel/gain change 16µs / channel in sequencer mode
Accuracy	±2 LSB @ 25°C with correction
Linearity	±2 LSB @ 25°C with correction
ADC INL/DNL Error	±3 LSB
Analog Output	
Number of Analog Outputs	8 analog output channels
Output Voltage Range	±10V
Correction Data	D/A Correction data for gain and offset stored in EEPROM
Resolution	16 bit
Conversion Time	10µs max.
Accuracy	±1 LSB @ 25°C with correction
Linearity	±2 LSB @ 25°C with correction
DAC INL/DNL Error	±4/±3 LSB
Capacitive Load	Up to 10 000pF

Digital I/O		
Number of Digital I/O	16 digital I/O channels	
Minimum Pulse Width (Input)	Programmable, 100ns – 6.55ms	
I/O Interface		
I/O Connector	Front I/O: HD68 SCSI-3 type female connector (AMP 787082-7) No PMC P14 I/O	
Physical Data		
Power Requirements	250 mA typical @ +5V DC	
Temperature Range	Operating Storage	-40°C to +85 °C -40°C to +85°C
MTBF	213573 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	75.4 g	

Table 2-1 : Technical Specification

3 Handling and operation Instructions

3.1 ESD Protection

This PMC module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done with appropriate care.

4 Addressing

4.1 PCI Configuration Space

PCI CFG Register Address	Write '0' to all unused (Reserved) bits								PCI writeable	Initial Values (Hex Values)
	31	24	23	16	15	8	7	0		
0x00	Device ID				Vendor ID				N	0353 1498
0x04	Status				Command				Y	0280 0000
0x08	Class Code						Revision ID		N	118000 00
0x0C	not supported		Header Type		not supported		not supported		Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers								Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers								Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0								Y	FFFFFE00
0x1C	PCI Base Address 3 for Local Address Space 1								Y	FFFFFFC0
0x20	PCI Base Address 4 for Local Address Space 2								Y	FFFFFFC0
0x24	not supported								Y	00000000
0x28	not supported								N	00000000
0x2C	Subsystem ID				Subsystem Vendor ID				N	000A 1498
0x30	not supported								Y	00000000
0x34	Reserved						Cap. Ptr.		N	000000 40
0x38	Reserved								N	00000000
0x3C	Max_Lat		Min_Gnt		Interrupt Pin		Interrupt Line		Y[7:0]	00 00 01 00
0x40-0xFF	Reserved									00000000

Table 4-1 : PCI Controller Header

4.1.1 PCI Address Space Overview

PCI BAR	PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	0x10	MEM	128	32	Little	PCI Controller Register Space
1	0x14	I/O	128	32	Little	
2	2 (0x18)	MEM	512	32	BIG	Local Register Address Space
3	3 (0x1C)	MEM	64	16	BIG	Sequencer Data RAM
4	4 (0x20)	MEM	64	16	BIG	ADC/DAC Correction Data ROM
5	5 (0x24)	-	-	-	-	Not Used

Table 4-2 : PCI Address Space Overview

4.1.2 Configuration EEPROM

The serial EEPROM memory contains by default the TEWS PCI Interface FPGA configuration data for compatibility reasons. However, the entire configuration data is stored within and loaded from the internal flash of the PCI target chip.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x0353	0x1498	0x0280	0x0000	0x1180	0x0000	s.b.	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x4801	0x0000	0x0000
0x20	0x0000	0x4C06	0x0000	0x0003	0xFFFF	0xFE00	0xFFFF	0xFFC0
0x30	0xFFFF	0xFFC0	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x0201	0x0000	0x0301	0x0000	0x0000	0x0000	0x0000
0x50	0x0180	0x6022	0x0140	0x0022	0x0140	0x0022	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0101	0x0000	0x0221	0x0000	0x0321
0x70	0x0000	0x0000	0x0030	0x0041	0x0078	0x4000	0x026D	0xB6D2
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 4-3 : Configuration EEPROM TPMC851-10R

Subsystem-ID Value (Offset 0x0C): TPMC851-10R 0x000A

4.2 PCI Controller Register Space

4.2.1 PCI Controller Configuration Register Map

The PCI base address for the PCI Controller Configuration Registers is PCI Base Address 0 (PCI Memory Space, Offset 0x10 in the PCI Configuration Space) or PCI Base Address 1 (PCI I/O Space, Offset 0x14 in the PCI Configuration Space).

Do not change hardware dependent bit settings in the PCI Controller Configuration Registers.

Offset from PCI Base Address	Register	Value
0x00	Local Address Space 0 Range	0xFFFF_FE00
0x04	Local Address Space 1 Range	0xFFFF_FFC0
0x08	Local Address Space 2 Range	0xFFFF_FFC0
0x0C	Local Address Space 3 Range	0x0000_0000
0x10	Expansion ROM Range	0x0000_0000
0x14	Local Address Space 0 Local Base Address (Remap)	0x0000_0001
0x18	Local Address Space 1 Local Base Address (Remap)	0x0000_0201
0x1C	Local Address Space 2 Local Base Address (Remap)	0x0000_0301
0x20	Local Address Space 3 Local Base Address (Remap)	0x0000_0000
0x24	Expansion ROM Local Base Address (Remap)	0x0000_0000
0x28	Local Address Space 0 Bus Region Descriptor	0x0180_6022
0x2C	Local Address Space 1 Bus Region Descriptor	0x0140_0022
0x30	Local Address Space 2 Bus Region Descriptor	0x0140_0022
0x34	Local Address Space 3 Bus Region Descriptor	0x0000_0000
0x38	Expansion ROM Bus Region Descriptor	0x0000_0000
0x3C	Chip Select 0 Base Address	0x0000_0101
0x40	Chip Select 1 Base Address	0x0000_0221
0x44	Chip Select 2 Base Address	0x0000_0321
0x48	Chip Select 3 Base Address	0x0000_0000
0x4C	Interrupt Control/Status	0x0041
0x4E	Serial EEPROM Write-Protected Address Boundary	0x0030
0x50	PCI Target Response, Serial EEPROM Control, and Initialization Control	0x0078_4000
0x54	General Purpose I/O Control	0x026D_B6D2
0x70	Hidden1 Register for Power Management Data Select	0x0000_0000
0x74	Hidden 2 Register for Power Management Data Scale	0x0000_0000

Table 4-4 : PCI Controller Configuration Register Map

4.3 Local Register Address Space

The PCI base address for the Local Registers is PCI Base Address 2 (PCI Memory Space, Offset 0x18 in the PCI Configuration Space).

The register offsets stated below refer to 32 bit accesses. Registers shorter than 32 bit are filled with zeros on long word read-accesses. The not used addresses will return 0 when read.

Offset to PCI Base Address 2	Symbol	Register Name
0x0000	ADCCONT	ADC Control Register
0x0004	ADCDATA	ADC Data Register
0x0008	ADCSTAT	ADC Status Register
0x000C	ADCCONV	ADC Conversion Start Register
0x0010	ADCSEQCONT	ADC Sequencer Control Register
0x0014	ADCSEQSTAT	ADC Sequencer Status Register
0x0018	ADCSEQTIME	ADC Sequencer Timer Register
0x001C	ADCSETTLING	ADC Settling Time Register
0x0020 – 0x009C	ADCSEQIRAM	ADC Sequencer Instruction RAM 1-32
0x00A0 – 0x00BF	-	Not used
0x00C0	DACCONT	DAC Control Register
0x00C4	DACSEQSTAT	DAC Sequencer Status Register
0x00C8	DACSEQTIME	DAC Sequencer Timer Register
0x00CC	-	Not used
0x00D0 – 0x00EC	DACDATA	DAC Data Register 1-8
0x00F0 – 0x00FF	-	Not used
0x0100	LINEDIR	Line Direction Register
0x0104	LINEDEB	Line Debounce Enable Register
0x0108	LINEDBT	Line Debounce Time Register
0x010C	LINEIN	Line Input Register
0x0110	LINEOUT	Line Output Register
0x0114	LINEIEN	Line Interrupt Enable Register
0x0118	LINEIST	Line Interrupt Status Register
0x011C	-	Not used
0x0120	CNTPRL	Counter 1 Preload Register
0x0124	CNTCMP	Counter 1 Compare Register
0x0128	CNTDATA	Counter 1 Data Register
0x012C	CNTCONT	Counter 1 Control Register
0x0130	CNTSTAT	Counter 1 Status Register
0x0134	CNTCOM	Counter 1 Command Register
0x0138 – 0x013F	-	Not used
0x0140	ICR	Interrupt Control Register
0x0144 – 0x014F	-	Factory use only. Do not Write.
0x0150	CNTPRL_EXT	Counter 2 Preload Register
0x0154	CNTCMP_EXT	Counter 2 Compare Register

Offset to PCI Base Address 2	Symbol	Register Name
0x0158	CNTDATA_EXT	Counter 2 Data Register
0x015C	CNTCONT_EXT	Counter 2 Control Register
0x0160	CNTSTAT_EXT	Counter 2 Status Register
0x0164	CNTCOM_EXT	Counter 2 Command Register
0x0168-0x01F0	-	Reserved
0x01F4	BOARD_TEMP	Temperature Register
0x01F8	BOARD_SCRATCH	Scratchpad Register
0x01FC	BOARD_FIRM	Firmware Identification Register

Table 4-5 : Local Register Address Space

4.3.1 Analog Input Registers

4.3.1.1 ADC Control Register ADCCONT (Offset 0x0000)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:12</td><td>-</td><td>Reserved
Write: don't care
Read: always reads as '0'</td><td>R</td><td>0</td></tr>
<tr><td>11</td><td>RST</td><td>ADC Reset
If RST is set to ‘1’, the ADC is reset. Current conversions are aborted.
This bit is cleared immediately after a write access</td><td>R/W</td><td>0</td></tr>
<tr><td>10</td><td>IRQC</td><td>IRQ after Conversion Enable
0 = IRQ after Conversion disabled
1 = IRQ after Conversion enabled
An interrupt will be generated after a conversion is finished (ADC_BUSY changes from 1 to 0).
For pending interrupts and interrupt acknowledge see the ADC Status Register ADCSTAT.</td><td>R/W</td><td>0</td></tr>
<tr><td>9</td><td>IRQST</td><td>IRQ after Settling Time Enable
0 = IRQ after Settling Time disabled
1 = IRQ after Settling Time enabled
An interrupt will be generated after the settling time has elapsed (SETTL_BUSY changes from 1 to 0)
For pending interrupts and interrupt acknowledge see the ADC Status Register ADCSTAT.</td><td>R/W</td><td>0</td></tr>
<tr><td>8</td><td>ASTC</td><td>Automatic Settling Time Control
0 = OFF (Normal Mode)
A conversion must be initiated manually in the ADC Conversion Start Register ADCCONV.
1 = ON (Automatic Mode)
A conversion is automatically initiated after the settling time has elapsed.
The ADC settling time is appr. 16µs.</td><td>R/W</td><td>0</td></tr>
<tr><td>7:6</td><td>GAIN [1:0]</td><td>Gain Selection (Analog Input Amplifier)
<table>
<tr><th>GAIN1</th><th>GAIN0</th><th>Gain Factor</th><th>Input Voltage Range</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>±10V</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>±5V</td></tr>
<tr><td>1</td><td>0</td><td>4</td><td>±2.5V</td></tr>
<tr><td>1</td><td>1</td><td>8</td><td>±1.25V</td></tr>
</table></td><td>R/W</td><td>00</td></tr>
<tr><td>5</td><td>SE/DIFF</td><td>Single/Differential Mode Control
0 = Single-ended mode
32 single-ended input channels available
1 = Differential mode
16 differential input channels available</td><td>R/W</td><td>0</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>4:0</td><td>CS[4:0]</td><td>Channel Select (Analog Input Channel)
<table>
<tr><th>CS[4:0]</th><th>Single-ended Channel
SE/DIFF = 0</th><th>Differential Channel
SE/DIFF = 1</th></tr>
<tr><td>00000</td><td>CH1</td><td>CH1</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>01111</td><td>CH16</td><td>CH16</td></tr>
<tr><td>10000</td><td>CH17</td><td>N/A</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>11111</td><td>CH32</td><td>N/A</td></tr>
</table>
‘N/A’ = ADC Input connected to GND</td><td>R/W</td><td>00000</td></tr>
</table>

Table 4-6 : ADC Control Register

A write to this register sets the new channel and gain. Subsequent write accesses are ignored until the settling time has elapsed. This register is developed for a word (16 bit) or long word (32 bit) read/write access. Byte accesses on this register are not supported and will fail.

Do NOT write to this register while the sequencer is running! A write to this register while the sequencer is running can lead to unpredictable results!

Interrupts are generated only if the Master Interrupt Enable (MIE) is enabled in the Interrupt Control Register ICR.

4.3.1.2 ADC Data Register ADCDATA (Offset 0x0004)

The ADC Data Register contains the converted data value. The output format is two’s complement.

This register is updated if the conversion was initiated with the ADC Conversion Start Register ADCCONV or by the Automatic Settling Time Control ASTC on the falling edge of ADC_BUSY in the ADC Status Register (ADCSTAT). Conversions initiated by the sequencer will have no effect to this register.

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved Write: don't care Read: always reads as '0'	R	0
15:0		Stores the converted 16 bit data value.	R	0

Table 4-7 : ADC Data Register

Description	±10V (Gain 1)	±5V (Gain 2)	±2.5V (Gain 4)	±1.25V (Gain 8)	Two's Complement
Full Scale Range	±10V	±5V	±2.5	±1.25	
Least Significant Bit	305.2µV	152.6µV	76.2µV	38.15µV	
FSR - 1LSB	9.999695V	4.999847V	2.499924V	1.249962V	0x7FFF[1]
Midscale + 1LSB	305.2µV	152.6µV	76.2µV	38.15µV	0x0001
Midscale	0V	0V	0V	0V	0x0000
Midscale – 1LSB	-305.2µV	-152.6µV	-76.2µV	-38.15µV	0xFFFF
-FSR + 1LSB	-9.999695V	-4.999847V	-2.499924V	-1.249962V	
Full Scale (neg.)	-10V	-5V	-2.5V	1.25V	0x8000[2]

[1]This is also the code for an overrange analog input.
[2]This is also the code for an underrange analog input.

Table 4-8 : ADC Data Coding

After power up the on board ADC device is in a random state and requires two dummy conversions before operating correctly. This is based on the chip design of the ADC device.

Software should ignore the data of the first two ADC conversions after power-up.

The software drivers from TEWS Technologies already include these two dummy conversions.

4.3.1.3 ADC Status Register ADCSTAT (Offset 0x0008)

Bit	Symbol	Description	Access	Reset Value
31:4	-	Reserved Write: don't care Read: always read as '0'	R	0
3	SETTL IRQ	Pending Settling Time Interrupts (Read), Interrupt acknowledge (Write) On a read-access this bit shows a pending Settling Time interrupt. Pending interrupts are marked with a '1'. An interrupt is acknowledged by writing a '1' to this bit after the error flags are cleared.	R/C	0
2	ADC IRQ	Pending Conversion Interrupts (Read), Interrupt acknowledge (Write) On a read-access this bit shows a pending Conversion interrupt. Pending interrupts are marked with a '1'. An interrupt is acknowledged by writing a '1' to this bit after the error flags are cleared.	R/C	0
1	SETTL BUSY	SETTL_BUSY Indicates that the required settling time after a write to the CONTREG register is not yet done. This bit is set by writing to the CONTREG register. The bit is cleared when the required settling time has elapsed. This bit must be read as '0' before a conversion is started by a write to the ADC Conversion Start Register ADCCONV. The ADC settling time is appr. 16µs.	R	0
0	ADC BUSY	ADC_BUSY Indicates if an actual data conversion is in progress. If "Automatic Settling Time Mode" is OFF, this bit is set by writing to the ADC Conversion Start Register ADCCONV. If “Automatic Settling Time Mode” is ON, this bit is set automatically after the settling time has elapsed. This bit must be read as '0' before the conversion data is read from the DATAREG register.	R	0

Table 4-9 : ADC Status Register

Interrupts are generated only if the Master Interrupt Enable (MIE) is enabled in the Interrupt Control Register ICR.

4.3.1.4 ADC Conversion Start Register ADCCONV (Offset 0x000C)

The ADC Conversion Start Register is used to start an ADC conversion when “Automatic Settling Time Mode” is OFF. Any write access starts the conversion. The user must read the SETTL_BUSY bit in the ADC Status Register as '0' or wait for a Settling Time Interrupt before the conversion is started. The ADC_BUSY bit in the ADC Status Register indicates if the conversion data in the ADC Data Register is valid (ADC_BUSY bit = '0').

It is allowed to set up a new channel/gain by writing to the ADC Control Register CONTREG immediately after starting an ADC conversion.

If "Sequencer Mode" is selected (SEQCONT register bit 0 is set to '1') all write accesses to the ADC Conversion Start Register ADCCONV are ignored.

Please pay attention to the chapter "Important Notes".

4.3.1.5 ADC Sequencer Control Register ADCSEQCONT (Offset 0x0010)

Bit	Symbol	Description	Access	Reset Value
31:3	-	Reserved Write: don't care Read: always reads as '0'	R	0
2	SEQ INT ENA	Sequencer Interrupt Enable Control 0 = Sequencer Interrupt Disabled 1 = Sequencer Interrupt Enabled An interrupt request will be generated if any error flag is set in the ADCSEQSTAT Register (Sequencer Data Valid or Sequencer Error). For pending interrupts and interrupt acknowledge see ADC Sequencer Status Register ADCSEQSTAT.	R/W	0
1	SEQ TRIG	Sequencer Trigger Source 0 = Sequencer Timer 1 = External Signal (Dig I/O Line 0)	R/W	0
0	SEQ ON	Sequencer Start / Stop Control 0 = Stops the Sequencer after last Instruction (Sequencer Continuous Mode: Sequencer stops immediately). No DATA AV will be issued. 1 = Starts the Sequencer immediately	R/W	0

Table 4-10 : ADC Sequencer Control Register

If an error flag (DATA_OVERFLOW_ERROR, TIMER_ERROR, I-RAM_ERROR) is set in the Sequencer Status Register SEQSTAT, the sequencer will be stopped after the last instruction (SEQ_ON will be set to '0'). The user must clear the status bits and start the sequencer again.

Interrupts are generated only if the Master Interrupt Enable (MIE) is enabled in the Interrupt Control Register ICR.

Please pay attention to the chapter "Important Notes" before using the sequencer.

If ADC_OUT in the Line Direction Register LINEDIR is set to '1', the trigger signal for the sequencer is available for external use on Dig I/O Line 0.

Do not use the External Signal as Sequencer Trigger Source if ADC_OUT is enabled. This will cause the sequencer to lock.

4.3.1.6 ADC Sequencer Status Register ADCSEQSTAT (Offset 0x0014)

Bit	Symbol	Description	Access	Reset Value
31:5	-	Reserved Write: don't care Read: always reads as '0'	R	0
4	SEQ IRQ	Pending Sequencer Interrupts (Read), On a read-access this bit shows a pending Sequencer interrupt. Pending interrupts are marked with a '1'. An interrupt is acknowledged when the error flags are cleared.	R	0
3	I-RAM ERROR	Instruction RAM Error Flag Set by the sequencer if the sequencer has been started and there is no instruction in the Sequencer Instruction RAM. To clear this flag the user must write ‘1’ to this bit.	R/C	0
2	TIMER ERROR	Timer Error Flag Set by the sequencer if the sequencer timer has elapsed but the actual sequence is still in progress. To clear the Timer Error Flag the user must write ‘1’ to this bit. If the Sequencer Timer Register is 0 (Sequencer Continuous Mode) the Timer Error Flag always reads as ‘0’.	R/C	0
1	DATA OVERFLOW ERROR	Data Overflow Error Flag Set by the sequencer if the last sequencer instruction is done and the Data Available Flag of the previous sequence has not yet been cleared by the user. To clear the error flag the user must write ‘1’ to this bit. If the Sequencer Timer Register is 0 (Sequencer Continuous Mode) the Data Overflow Error Flag always reads as ‘0’.	R/C	0
0	DATA AV	Data Available Flag Set if a sequence is done and new ADC Data is available in the ADC Data RAM. After reading the ADC Data RAM the user must clear the Data Available Flag by writing ‘1’ to this bit.	R/C	0

Table 4-11 : ADC Sequencer Status Register

Description	Sequencer Timer	Continuous Mode	External Trigger
Data Available Flag	Active, IRQ	Active, no IRQ	Active, IRQ
Data Overflow Error Flag	Active, IRQ	Disabled	Active, IRQ
Timer Error Flag	Active, IRQ	Disabled	Active, IRQ
Instruction RAM Error Flag	Active, IRQ	Active, IRQ	Active, IRQ

Table 4-12 : Error Flag IRQ generation

Also see chapter ‘Sequencer Errors’ for details.

4.3.1.7 ADC Sequencer Timer Register ADCSEQTIME (Offset 0x0018)

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved Write: don't care Read: always reads as '0'	R	0
15:0		Sequencer Timer Preload Value	R/W	0

Table 4-13 : ADC Sequencer Timer Register

The Sequencer Timer is programmable from 100µs to 6.5535s in 100µs steps. The time base for the sequencer timer is derived from an on board 40 MHz oscillator.

Whenever the timer reaches the programmed value the sequencer starts a new sequence with the first instruction found in the instruction RAM.

Assure that the time needed to complete a sequence is suitable to the chosen sequence timer value. If the sequence timer elapses while a sequence is still in progress, a timer error will be asserted.

If the Sequencer Timer Register is set to '0', the "Sequencer Continuous Mode" is selected. The sequencer will start again with the first instruction of the sequence immediately after the last instruction of the previous sequence has been completed. In this mode the Timer Error Flag (TIMER_ERROR) and the Data Overflow Error Flag (DATA_OVERFLOW_ERROR) are not active and will read as '0'. The Data Available Flag (DATA_AV) will be active, but will not produce an interrupt.

4.3.1.8 ADC Settling Time Register ADCSETTLING (Offset0x001C)

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved Write: don't care Read: always reads as '0'	R	0
15:0	ADCSETT	ADC Settling Time = ADCSETT * 25 ns The reset value corresponds to the default recommended settling time 0x280 = 16 us	R/W	0x0280

Table 4-14 : ADC Settling Time Register

Register values less than 0x0100 (the minimum required settling time of ca. 6.4 us) will be ignored and the register will be reset to its default value.

4.3.1.9 ADC Sequencer Instruction RAM (Offset 0x0020 - Offset 0x009C)

Bit	Symbol	Description	Access	Reset Value
31:4	-	Reserved Write: don't care Read: always reads as '0'	R	0
3:2	GAIN [1:0]	Gain Selection (Analog Input Amplifier)	R/W	00
1	ENA	Enable this ADC Channel for the Sequencer	R/W	0

GAIN1	GAIN0	Gain Factor	Input Voltage Range
0	0	1	±10V
0	1	2	±5V
1	0	4	±2.5V
1	1	8	±1.25V

		0 = Sequencer will pass over the ADC Channel 1 = Sequencer converts this ADC Channel and updates the ADC Data in the Sequencer Data RAM at the end of the sequence.		
0	SE/DIFF	Single/Differential Mode Control 0 = Single-ended mode 32 single ended channels available 1 = Differential mode 16 differential channels available. Only channels 1-16 can be configured as differential channel. Channels 17 to 32 are used as input for channels 1 to 16.	R/W	0

Table 4-15 : ADC Sequencer Instruction RAM Register

If a channel is configured as differential channel, the instruction of the associated channel is ignored (see following chart or chapter 'Pin Assignment – I/O Connector' for the associated channels).

Within a sequence mixed single-ended and differential modes are possible.

Example: Channel 1 to channel 8 (with channels 17 to channel 24) are selected as differential inputs, channel 9 to channel 16 and channel 25 to channel 32 as single-ended input channels.

Only the Sequencer Data RAM locations of channels enabled for the sequence are updated at the end of a sequence. All other RAM locations are empty or contain old data.

Example: If only channel 1, channel 2, and channel 8 are enabled, only the three ADC RAM locations for channel 1, channel 2, and channel 8 are updated at the end of the sequence. The user must only read these three ADC RAM locations then.

If a sequence is started with an empty instruction RAM, an I-RAM error is issued.

The Sequencer Instruction RAM is accessible only while the sequencer is not running (SEQ_ON = 0).

The following table shows the position of the Sequencer Instruction RAM bytes in the local memory space.

Offset	Single Ended	Differential
0x20	Channel 1	Channel 1
0x24	Channel 2	Channel 2
0x28	Channel 3	Channel 3
0x2C	Channel 4	Channel 4
0x30	Channel 5	Channel 5
0x34	Channel 6	Channel 6
0x38	Channel 7	Channel 7
0x3C	Channel 8	Channel 8
0x40	Channel 9	Channel 9
0x44	Channel 10	Channel 10
0x48	Channel 11	Channel 11
0x4C	Channel 12	Channel 12
0x50	Channel 13	Channel 13
0x54	Channel 14	Channel 14
0x58	Channel 15	Channel 15
0x5C	Channel 16	Channel 16
0x60	Channel 17	N/A (Input for Channel 1)
0x64	Channel 18	N/A (Input for Channel 2)
0x68	Channel 19	N/A (Input for Channel 3)
0x6C	Channel 20	N/A (Input for Channel 4)
0x70	Channel 21	N/A (Input for Channel 5)
0x74	Channel 22	N/A (Input for Channel 6)
0x78	Channel 23	N/A (Input for Channel 7)
0x7C	Channel 24	N/A (Input for Channel 8)
0x80	Channel 25	N/A (Input for Channel 9)
0x84	Channel 26	N/A (Input for Channel 10)
0x88	Channel 27	N/A (Input for Channel 11)
0x8C	Channel 28	N/A (Input for Channel 12)
0x90	Channel 29	N/A (Input for Channel 13)
0x94	Channel 30	N/A (Input for Channel 14)
0x98	Channel 31	N/A (Input for Channel 15)
0x9C	Channel 32	N/A (Input for Channel 16)

Table 4-16 : ADC Sequencer Instruction RAM Register positions

4.3.2 Analog Output Registers

4.3.2.1 DAC Control Register DACCONT (Offset 0x00C0)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:6</td><td>-</td><td>Reserved
Write: don't care
Read: always reads as '0'</td><td>R</td><td>0</td></tr>
<tr><td>5</td><td>DAC IRQ ENA</td><td>DAC Interrupt Enable
0 = DAC Interrupt Disabled
1 = DAC Interrupt Enabled
An interrupt is issued on a Sequencer Data Request in the Sequencer Update or Trigger Update mode.
For pending interrupts and interrupt acknowledge see DAC Sequencer Status Register DACSEQSTAT.</td><td>R/W</td><td>0</td></tr>
<tr><td>4:3</td><td>LOAD SEL</td><td>Load Mode Select
The Load Mode determines how the DAC outputs are updated.
<table>
<tr><th>LOADSEL[1:0]</th><th>Load Mode</th></tr>
<tr><td colspan="2">Immediate Update</td></tr>
<tr><td>00</td><td>Immediate Update:
The DAC outputs are updated immediately on a write access to a DAC Data Register.</td></tr>
<tr><td colspan="2">Simultaneous Update</td></tr>
<tr><td>01</td><td>Manual Update:
All DAC outputs are updated simultaneously when LOADDAC is set to ‘1’.</td></tr>
<tr><td>10</td><td>Sequencer Update:
All DAC outputs are updated simultaneously when the DAC Sequencer Timer reaches zero.</td></tr>
<tr><td>11</td><td>Trigger Update:
All DAC outputs are updated simultaneously by an external trigger (Dig I/O Line 1).</td></tr>
</table>
In the Simultaneous Update modes it is required to load the DACs with data via the DAC Data Registers. This data is buffered until the trigger event on which all DACs are updated simultaneously with the buffered data. If a channel was not loaded with new data, it will use the old data previously buffered.</td><td>R/W</td><td>0</td></tr>
<tr><td>2</td><td>LOAD DAC</td><td>In Manual Update mode writing a ‘1’ loads all DACs simultaneously. This bit is cleared immediately after a write access.</td><td>W</td><td>0</td></tr>
<tr><td>1</td><td>RSTSEL</td><td>Reset Select.
Indicates the action of RSTDAC. A RSTDAC command will set the DAC registers and outputs to midscale.
Hardwired to ‘1’</td><td>R</td><td>1</td></tr>
<tr><td>0</td><td>RSTDAC</td><td>Reset DACs
Writing ‘1’ resets the DACs. The DACs are set to midscale. This bit is cleared immediately after a write access.</td><td>W</td><td>0</td></tr>
</table>

Table 4-17 : DAC Control Register

DAC analog outputs of all channels are held in a reset state for the time of a PCI or local reset.

Interrupts are generated only if the Master Interrupt Enable (MIE) is enabled in the Interrupt Control Register ICR.

If DAC_OUT in the Line Direction Register LINEDIR is set to ‘1’, the trigger signal for the sequencer is available for external use on Dig I/O Line 1.

Do not use the Trigger Update mode if DAC_OUT is enabled. This would cause the sequencer to lock.

4.3.2.2 DAC Sequencer Status Register DACSEQSTAT (Offset 0x00C4)

Bit	Symbol	Description	Access	Reset Value
31:3	-	Reserved Write: don't care Read: always reads as '0'	R	0
2	DAC IRQ	Pending DAC Interrupts (Read), On a read-access this bit shows a pending DAC interrupt. Pending interrupts are marked with a '1'. An interrupt is acknowledged when the SDR bit is cleared.	R	0
1	SDU	Sequencer Data Underflow (bit is used to signalize a data underflow condition for the sequencer data RAM) 1 = Sequencer Data Underflow (sequencer is ready for the next sequence but the user has not yet confirmed new data in sequencer data RAM). 0 = All DAC Data Registers have been updated with new data.	R	1
0	SDR	Sequencer Data Request/Acknowledge (bit is used to signalize data request for the sequencer data RAM) 1 = Sequencer Data Request (sequencer is requesting new data in the sequencer data RAM) During the Simultaneous/Sequencer/Trigger Update modes this status bit must be cleared after the sequencer data RAM has been updated with data for the next sequence. The bit is cleared by writing a '1'.	R/C	0

Table 4-18 : DAC Sequencer Status Register

4.3.2.3 DAC Sequencer Timer Register DACSEQTIME (Offset 0x00C8)

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved Write: don't care Read: always reads as '0'	R	0
15:0		Sequencer Timer Preload Value	R/W	0

Table 4-19 : DAC Sequencer Timer Register

Setting LOADSEL in the DAC Control Register (DACCONT) to ‘Sequencer Update’ starts the timer. The minimum for the Sequencer Timer Preload Value is 1; the timer will not start if the Sequencer Timer Preload Value is 0.

The sequencer timer is programmable from 100µs to 6.5535s in 100µs steps. The sequencer timer is loaded with the value in the Sequencer Timer Register when a sequence is started. In sequencer timer mode the start of the next sequence is delayed for: Register Value * 100µs.

The time base for the sequencer timer is derived from an on board 40 MHz oscillator.

4.3.2.4 DAC Data Register DACDATA 1-8 (Offset 0x00D0 - Offset 0x00EC)

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved Write: don't care Read: always reads as '0'	R	0
15:0	DAC DATA 1-8	DAC Data Value When LOADSEL in the DAC Control Register is set to “00”, the DAC output is updated immediately.	R/W	0x0000

Table 4-20 : DAC Data Register

After power-on or reset the value of all DAC Data registers are set to 0x8000. The analog output voltage is set to Midscale 0V DC.

The settling time for a full range voltage step is typically 8µs and maximum 10µs.

Description	Output Voltage	DAC Data Value (in two’s complement)
Full Scale Range	±10V	
Least Significant Bit	305.2µV	
FSR - 1LSB	9.999695V	0x7FFF
Midscale + 1LSB	305.2µV	0x0001
Midscale	0V	0x0000
Midscale – 1LSB	-305.2µV	0xFFFF
-FSR + 1LSB	-9.999695V	0x8001
Full Scale (neg.)	-10V	0x8000

Table 4-21 : DAC Data Coding

4.3.3 Digital I/O Registers

4.3.3.1 Line Direction Register LINEDIR (Offset 0x0100)

Bit	Symbol	Description		Access	Reset Value
31:18	-	Reserved Write: don't care Read: always reads as '0'		R	0
17	DAC OUT	Enable DAC Sequencer trigger output 1 = Override LINEDIR1 and output DAC Sequencer trigger on I/O Line 1 0 = Normal LINEDIR1 operation		R/W	0
16	ADC OUT	Enable ADC Sequencer trigger output 1 = Override LINEDIR0 and output ADC Sequencer trigger on I/O Line 0 0 = Normal LINEDIR0 operation		R/W	0
15	LINEDIR15	I/O Line 15	0 = TTL I/O line as Input 1 = TTL I/O line as Output	R/W	0
14	LINEDIR14	I/O Line 14			0
13	LINEDIR13	I/O Line 13			0
12	LINEDIR12	I/O Line 12			0
11	LINEDIR11	I/O Line 11			0
10	LINEDIR10	I/O Line 10			0
9	LINEDIR9	I/O Line 9			0

8	LINEDIR8	I/O Line 8			0
7	LINEDIR7	I/O Line 7			0
6	LINEDIR6	I/O Line 6			0
5	LINEDIR5	I/O Line 5			0
4	LINEDIR4	I/O Line 4			0
3	LINEDIR3	I/O Line 3			0
2	LINEDIR2	I/O Line 2			0
1	LINEDIR1	I/O Line 1			0
0	LINEDIR0	I/O Line 0			0

Table 4-22 : Line Direction Register

The reset value of the Line Direction Register is 0x0000. That means all TTL I/O lines are inputs.

4.3.3.2 Line Debounce Enable Register LINEDEB (Offset 0x0104)

Bit	Symbol	Description		Access	Reset Value
31:16	-	Reserved Write: don't care Read: always reads as '0'		R	0
15	LINEDEB15	I/O Line 15		R/W	0
14	LINEDEB14	I/O Line 14			0
13	LINEDEB13	I/O Line 13			0
12	LINEDEB12	I/O Line 12			0
11	LINEDEB11	I/O Line 11			0
10	LINEDEB10	I/O Line 10			0
9	LINEDEB9	I/O Line 9			0
8	LINEDEB8	I/O Line 8	0 = Debounce disabled for this TTL I/O line 1 = Debounce enabled for this TTL I/O line		0
7	LINEDEB7	I/O Line 7			0
6	LINEDEB6	I/O Line 6			0
5	LINEDEB5	I/O Line 5			0
4	LINEDEB4	I/O Line 4			0
3	LINEDEB3	I/O Line 3			0
2	LINEDEB2	I/O Line 2			0
1	LINEDEB1	I/O Line 1			0
0	LINEDEB0	I/O Line 0			0

Table 4-23 : Line Debounce Enable Register

For the enabled I/O lines a digital debounce filter will be applied. The debounce duration can be programmed in the Line Debounce Time Register LINEDBT. The digital input signal must have duration greater than the programmed debounce duration in order to be recognized as a valid input signal.

The disabled I/O lines will not be filtered.

4.3.3.3 Line Debounce Time Register LINEDBT (Offset 0x0108)

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved Write: don't care Read: always reads as '0'	R	0
15:0		Line Debounce Time Value	R/W	0

Table 4-24 : Line Debounce Time Register

The Line Debounce Time Register allows to program the debounce duration from 100ns to 6.55ms. Use following formula to calculate the debounce duration:

Debounce duration = (Line Debounce Time Value * 100ns) + 100ns

The debounce time is common for all 16 inputs.

4.3.3.4 Line Input Register LINEIN (Offset 0x010C)

Bit	Symbol	Description		Access	Reset Value
31:16	-	Reserved Write: don't care Read: always reads as '0'		R	0
15	LINEIN15	I/O Line 15	Reflects the actual input state of the debounced TTL I/O lines at all times, including I/O lines configured as output in the LINEDIR (to provide readback functionality) 0 = TTL I/O line logic low 1 = TTL I/O line logic high	R	0
14	LINEIN14	I/O Line 14			0
13	LINEIN13	I/O Line 13			0
12	LINEIN12	I/O Line 12			0
11	LINEIN11	I/O Line 11			0
10	LINEIN10	I/O Line 10			0
9	LINEIN9	I/O Line 9			0
8	LINEIN8	I/O Line 8			0
7	LINEIN7	I/O Line 7			0
6	LINEIN6	I/O Line 6			0
5	LINEIN5	I/O Line 5			0
4	LINEIN4	I/O Line 4			0
3	LINEIN3	I/O Line 3			0
2	LINEIN2	I/O Line 2			0
1	LINEIN1	I/O Line 1			0
0	LINEIN0	I/O Line 0			0

Table 4-25 : Line Input Register

4.3.3.5 Line Output Register LINEOUT (Offset 0x0110)

Bit	Symbol	Description		Access	Reset Value
31:16	-	Reserved Write: don't care Read: always reads as '0'		R	0
15	LINEOUT15	I/O Line 15	Sets output state of the TTL I/O lines. Writes on I/O lines configured as input in the LINEDIR are allowed but will take no effect. 0 = TTL I/O line logic low 1 = TTL I/O line logic high	R/W	0
14	LINEOUT14	I/O Line 14			0
13	LINEOUT13	I/O Line 13			0
12	LINEOUT12	I/O Line 12			0
11	LINEOUT11	I/O Line 11			0
10	LINEOUT10	I/O Line 10			0
9	LINEOUT9	I/O Line 9			0
8	LINEOUT8	I/O Line 8			0
7	LINEOUT7	I/O Line 7			0
6	LINEOUT6	I/O Line 6			0
5	LINEOUT5	I/O Line 5			0
4	LINEOUT4	I/O Line 4			0
3	LINEOUT3	I/O Line 3			0
2	LINEOUT2	I/O Line 2			0
1	LINEOUT1	I/O Line 1			0
0	LINEOUT0	I/O Line 0			0

Table 4-26 : Line Output Register

4.3.3.6 Line Interrupt Enable Register LINEIEN (Offset 0x0114)

Bit	Symbol	Description		Access	Reset Value
31	LINEIENN15	I/O Line 15	0 = Disable Interrupt for negative transitions for I/O line 1 = Enable Interrupt for negative transitions for I/O line An interrupt will be generated when the input line changes from 1 to 0. For pending interrupts and interrupt acknowledge see the Line Interrupt Status Register LINEIST.	R/W	0
30	LINEIENN14	I/O Line 14			0
29	LINEIENN13	I/O Line 13			0
28	LINEIENN12	I/O Line 12			0
27	LINEIENN11	I/O Line 11			0
26	LINEIENN10	I/O Line 10			0
25	LINEIENN9	I/O Line 9			0
24	LINEIENN8	I/O Line 8			0
23	LINEIENN7	I/O Line 7			0
22	LINEIENN6	I/O Line 6			0
21	LINEIENN5	I/O Line 5			0
20	LINEIENN4	I/O Line 4			0
19	LINEIENN3	I/O Line 3			0
18	LINEIENN2	I/O Line 2			0
17	LINEIENN1	I/O Line 1			0
16	LINEIENN0	I/O Line 0			0
15	LINEIENP15	I/O Line 15	0 = Disable interrupt for positive transitions for I/O line 1 = Enable interrupt for positive transitions for I/O line An interrupt will be generated when the input line changes from 0 to 1. For pending interrupts and interrupt acknowledge see the Line Interrupt Status Register LINEIST.	R/W	0
14	LINEIENP14	I/O Line 14			0
13	LINEIENP13	I/O Line 13			0
12	LINEIENP12	I/O Line 12			0
11	LINEIENP11	I/O Line 11			0

10	LINEIENP10	I/O Line 10			0
9	LINEIENP9	I/O Line 9			0
8	LINEIENP8	I/O Line 8			0
7	LINEIENP7	I/O Line 7			0
6	LINEIENP6	I/O Line 6			0
5	LINEIENP5	I/O Line 5			0
4	LINEIENP4	I/O Line 4			0
3	LINEIENP3	I/O Line 3			0
2	LINEIENP2	I/O Line 2			0
1	LINEIENP1	I/O Line 1			0
0	LINEIENP0	I/O Line 0			0

Table 4-27 : Line Interrupt Enable Register

Interrupts are generated only if the Master Interrupt Enable (MIE) is enabled in the Interrupt Control Register ICR.

4.3.3.7 Line Interrupt Status Register LINEIST (Offset 0x0118)

Bit	Symbol	Description		Access	Reset Value
31	LINEISTN15	I/O Line 15	Interrupt status for negative transitions Read access: 0 : no interrupt request pending 1 : interrupt request pending Write access: 1 : clear pending interrupt request	R/C	0
30	LINEISTN14	I/O Line 14			0
29	LINEISTN13	I/O Line 13			0
28	LINEISTN12	I/O Line 12			0
27	LINEISTN11	I/O Line 11			0
26	LINEISTN10	I/O Line 10			0
25	LINEISTN9	I/O Line 9			0
24	LINEISTN8	I/O Line 8			0
23	LINEISTN7	I/O Line 7			0
22	LINEISTN6	I/O Line 6			0
21	LINEISTN5	I/O Line 5			0
20	LINEISTN4	I/O Line 4			0
19	LINEISTN3	I/O Line 3			0
18	LINEISTN2	I/O Line 2			0
17	LINEISTN1	I/O Line 1			0
16	LINEISTN0	I/O Line 0			0
15	LINEISTP15	I/O Line 15	Interrupt status for positive transitions Read access: 0 : no interrupt request pending 1 : interrupt request pending Write access: 1 : clear pending interrupt request	R/C	0
14	LINEISTP14	I/O Line 14			0
13	LINEISTP13	I/O Line 13			0
12	LINEISTP12	I/O Line 12			0
11	LINEISTP11	I/O Line 11			0
10	LINEISTP10	I/O Line 10			0
9	LINEISTP9	I/O Line 9			0
8	LINEISTP8	I/O Line 8			0
7	LINEISTP7	I/O Line 7			0
6	LINEISTP6	I/O Line 6			0
5	LINEISTP5	I/O Line 5			0
4	LINEISTP4	I/O Line 4			0

3	LINEISTP3	I/O Line 3			0
2	LINEISTP2	I/O Line 2			0
1	LINEISTP1	I/O Line 1			0
0	LINEISTP0	I/O Line 0			0

Table 4-28 : Line Interrupt Status Register

4.3.4 Counter 1 Registers

4.3.4.1 Counter 1 Preload Register CNTPRL (Offset 0x0120)

Bit	Symbol	Description	Access	Reset Value
31:0	CNTPRL	Counter 1 Preload Register The value of this register can be loaded into the counter by: - Setting bit 1 (LCNT) of the Channel Command Register - An impulse on the Control-Input when the 'Load on Control'-mode is active - Automatically in the 'Divide-by-N'-mode every time the counter creates a borrow or a carry	R/W	0

Table 4-29 : Counter 1 Preload Register

4.3.4.2 Counter 1 Compare Register CNTCMP (Offset 0x0124)

Bit	Symbol	Description	Access	Reset Value
31:0	CNTCMP	Counter 1 Compare Register Every time the counter matches Counter 1 Compare Register value, bit 2 (MAT) of Counter 1 Status Register is set to '1' and, if enabled, a Match Interrupt is generated.	R/W	-1

Table 4-30 : Counter 1 Compare Register

4.3.4.3 Counter 1 Data Register CNTDATA (Offset 0x0128)

Bit	Symbol	Description	Access	Reset Value
31:0	CNTDATA	Counter 1 Data Register This Register contains the actual Counter Data Value. A Latch Mode event loads the current counter value into this Register. The counter value is latched until Counter 1 Data Register is read or when bit 5 (CDLT) of Counter 1 Status Register is set to '1'.	R	0

Table 4-31 : Counter 1 Data Register

Counter 1 Data Register will not load again while the latch is active. If a Latch Mode event occurs while Counter 1 Data Register Latch is active, the OVFL bit in Counter 1 Status Register will be set to indicate that data was lost.

To avoid data inconsistencies this register is developed for a long word (32 bit) read/write access. Byte or word accesses on this register are not supported and will fail.

4.3.4.4 Counter 1 Control Register CNTCONT (Offset 0x012C)

Bit	Symbol	Description	Access	Reset Value
31:15	-	Reserved Write: don't care Read: always reads as '0'	-	0

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>14:12</td><td>POL</td><td>Input Polarity
The Input Polarity Control can be used to adapt the counter inputs to the input source polarity.
<table>
<tr><th>POL</th><th>Input</th><th>Polarity</th></tr>
<tr><td>14</td><td>TTL I/O line 4</td><td>0 = high active, 1 = low active</td></tr>
<tr><td>13</td><td>TTL I/O line 3</td><td>0 = high active, 1 = low active</td></tr>
<tr><td>12</td><td>TTL I/O line 2</td><td>0 = high active, 1 = low active</td></tr>
</table></td><td>R/W</td><td>000</td></tr>
<tr><td>11</td><td>CIEN</td><td>Enable Control Mode Interrupt
0 = Control Mode Interrupt disabled
1 = Control Mode Interrupt enabled
An interrupt will be generated on a control mode event.
For pending interrupts and interrupt acknowledge see Counter 1 Status Register CNTSTAT.</td><td>R/W</td><td>0</td></tr>
<tr><td>10</td><td>MIEN</td><td>Enable Match Interrupt
0 = Match Interrupt disabled
1 = Match Interrupt enabled
An interrupt will be generated when the counter value matches Counter 1 Compare Register CNTCMP.
For pending interrupts and interrupt acknowledge see Counter 1 Status Register CNTSTAT.</td><td>R/W</td><td>0</td></tr>
<tr><td>9:7</td><td>ZCM</td><td>Control Mode
The Control Mode determines how the counter interprets the Control Input (I/O line 4).
<table>
<tr><th>ZCM</th><th>Control Mode</th></tr>
<tr><td>000</td><td>No Control Mode</td></tr>
<tr><td>001</td><td>Load Mode</td></tr>
<tr><td>010</td><td>Latch Mode</td></tr>
<tr><td>011</td><td>Gate Mode</td></tr>
<tr><td>100</td><td>Reset Mode</td></tr>
</table>
See chapter ‘Control Modes’ for details.</td><td>R/W</td><td>000</td></tr>
<tr><td>6:5</td><td>SCM</td><td>Count Mode
The Count Mode determines the behavior of the counter.
<table>
<tr><th>SCM</th><th>Count Mode</th></tr>
<tr><td>00</td><td>Cycling Counter</td></tr>
<tr><td>01</td><td>Divide-by-N</td></tr>
<tr><td>10</td><td>Single Cycle</td></tr>
</table>
See chapter ‘Count Modes’ for details.</td><td>R/W</td><td>00</td></tr>
<tr><td>4:3</td><td>CLKDIV</td><td>Internal Clock Prescaler
<table>
<tr><th>CLKDIV</th><th>Prescaler</th><th>Clock frequency</th></tr>
<tr><td>00</td><td>1x</td><td>40 MHz</td></tr>
<tr><td>01</td><td>2x</td><td>20 MHz</td></tr>
<tr><td>10</td><td>4x</td><td>10 MHz</td></tr>
<tr><td>11</td><td>8x</td><td>5 MHz</td></tr>
</table></td><td>R/W</td><td>00</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>2:0</td><td>INPUT</td><td>Input Mode
The Input Mode determines the input source for the counter and how the counter interprets these input signals. The quadrature mode can be used with a 1x, 2x, or 4x resolution multiplier.
<table>
<tr><th>INPUT</th><th>Input Mode</th><th>Input Source</th></tr>
<tr><td>000</td><td>Counter disabled</td><td>-</td></tr>
<tr><td>001</td><td>Timer Mode Up</td><td>Internal Clock Prescaler</td></tr>
<tr><td>010</td><td>Timer Mode Down</td><td>Internal Clock Prescaler</td></tr>
<tr><td>011</td><td>Direction Count</td><td>I/O line 2 & 3</td></tr>
<tr><td>100</td><td>Up/Down Count</td><td>I/O line 2 & 3</td></tr>
<tr><td>101</td><td>Quadrature Count 1x</td><td>I/O line 2 & 3</td></tr>
<tr><td>110</td><td>Quadrature Count 2x</td><td>I/O line 2 & 3</td></tr>
<tr><td>111</td><td>Quadrature Count 4x</td><td>I/O line 2 & 3</td></tr>
</table>
See chapter ‘Input Modes’ for details.</td><td>R/W</td><td>000</td></tr>
</table>

Table 4-32 : Counter 1 Control Register

Interrupts are generated only if the Master Interrupt Enable (MIE) is enabled in the Interrupt Control Register ICR.

4.3.4.5 Counter 1 Status Register CNTSTAT (Offset 0x0130)

Bit	Symbol	Description	Access	Reset Value
31:10	-	Reserved Read: always reads as '0'	R	0
9	CIRQ	Pending Control Mode Interrupts (Read), Interrupt acknowledge (Write) On a read-access this bit shows a pending Control Mode Interrupt. Pending interrupts are marked with a '1'. An interrupt is acknowledged by writing a '1' to this bit.	R/C	0
8	MIRQ	Pending Match Interrupts (Read), Interrupt acknowledge (Write) On a read-access this bit shows a pending Match Interrupt. Pending interrupts are marked with a '1'. An interrupt is acknowledged when the MAT bit is cleared.	R	0
7	SGL	Single Cycle active In Single Cycle counting mode this bit is set to ‘1’ if the counter is enabled.	R	0
6	OVFL	Counter 1 Data Register Latch Overflow If a Latch Mode event occurs while Counter 1 Data Register Latch is active, this bit will be set to indicate that data was lost. This bit must be reset by writing a '1' to this bit.	R/C	0
5	CDLT	Counter 1 Data Register Latch This bit is set to '1', when Counter 1 Data Register is latched due to a 'Latch on Control. This bit is cleared after a read access to the Output Register or by writing a '1' to this bit.	R/C	0
4	DIR	Count Direction This bit indicates the direction, the counter is counting to. '1' indicates up, '0' indicates down. In the 'Up/Down Count' mode this bit indicates the direction at the last count. In the 'Direction Count' mode this bit corresponds to the Y-input.	R	0
3	SGN	Sign The Sign bit is set to '1' when the counter overflows, and set to '0' when the counter underflows.	R	0

		After reset or power-up this bit should be considered as "don't care" until the first Carry or Borrow occurred.		
2	MAT	Match This bit is set to '1' when the counter value matches the value of Counter 1 Compare Register. This bit must be reset by writing a '1' to this bit.	R/C	0
1	CRY	Carry This bit is set to '1' when the counter changes from 0xFFFFFFFF to 0x00000000. This bit must be reset by writing a '1' to this bit.	R/C	0
0	BOR	Borrow This bit is set to '1' when the counter changes from 0x00000000 to 0xFFFFFFFF. This bit must be reset by writing a '1' to this bit.	R/C	0

Table 4-33 : Counter 1 Status Register

4.3.4.6 Counter 1 Command Register CNTCOM (Offset 0x0134)

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved Write: don't care	-	-
1	LCNT	Load Counter Write '1' to load the counter with the value of Counter 1 Preload Register CNTPRL. This bit is cleared immediately after a write access.	W	0
0	RCNT	Reset Counter Write '1' to reset the counter. This bit is cleared immediately after a write access.	W	0

Table 4-34 : Counter 1 Command Register

4.3.5 Interrupt Control Register ICR (Offset 0x0140)

Bit	Symbol	Description	Access	Reset Value
31:10	-	Reserved Write: don't care Read: always reads as '0'	R	0
9	CIRQ_EXT	Pending Control Mode Interrupt 2 This interrupt must be acknowledged in Counter 2 Status Register CNTSTAT_EXT	R	0
8	MIRQ_EXT	Pending Match Interrupt 2 This interrupt must be acknowledged in Counter 2 Status Register CNTSTAT_EXT	R	0
7	CIRQ	Pending Control Mode Interrupt 1 This interrupt must be acknowledged in Counter 1 Status Register CNTSTAT	R	0
6	MIRQ	Pending Match Interrupt 1 This interrupt must be acknowledged in Counter 1 Status Register CNTSTAT	R	0
5	LINEIST	Pending Digital I/O Line IRQ This interrupt must be acknowledged in the Line Interrupt Status Register LINEIST	R	0
4	DAC IRQ	Pending DAC Sequencer Interrupt This interrupt must be acknowledged in the DAC Sequencer Status Register DACSEQSTAT	R	0
3	SEQ IRQ	Pending ADC Sequencer Interrupt This interrupt must be acknowledged in the ADC Sequencer Status Register ADCSEQSTAT	R	0
2	IRQST	Pending IRQ after Settling Time This interrupt must be acknowledged in the ADC Status Register ADCSTAT	R	0
1	IRQC	Pending IRQ after Conversion This interrupt must be acknowledged in the ADC Status Register ADCSTAT	R	0
0	MIE	Master Interrupt Enable 0 = All interrupts requests are disabled 1 = Interrupts requests are enabled	R/W	0

Table 4-35 : Interrupt Control Register

The interrupt flags in this register are informational only. All interrupts must be acknowledged in their associated registers.

Interrupts are generated only if the Master Interrupt Enable (MIE) is enabled in the Interrupt Control Register ICR.

4.3.6 Counter 2 Registers

4.3.6.1 Counter 2 Preload Register CNTPRL_EXT (Offset 0x0150)

Bit	Symbol	Description	Access	Reset Value
31:0	CNTPRL_EXT	Counter 2 Preload Register The value of this register can be loaded into the counter by: - Setting bit 2 (LCNT) of the Channel Command Register - An impulse on the Control-Input when the 'Load on Control'-mode is active - Automatically in the 'Divide-by-N'-mode every time the counter creates a borrow or a carry	R/W	0

Table 4-36 : Counter 2 Preload Register

4.3.6.2 Counter 2 Compare Register CNTCMP_EXT (Offset 0x0154)

Bit	Symbol	Description	Access	Reset Value
31:0	CNTCMP_EXT	Counter 2 Compare Register Every time the counter matches Counter 2 Compare Register value, bit 2 (MAT_EXT) of Counter 2 Status Register is set to '1' and, if enabled, a Match Interrupt is generated.	R/W	-1

Table 4-37 : Counter 2 Compare Register

4.3.6.3 Counter 2 Data Register CNTDATA_EXT (Offset 0x0158)

Bit	Symbol	Description	Access	Reset Value
31:0	CNTDATA_EXT	Counter 2 Data Register This Register contains the actual Counter Data Value. A Latch Mode event loads the current counter value into this Register. The counter value is latched until Counter 2 Data Register is read or when bit 5 (CDLT_EXT) of Counter 2 Status Register is set to '1'.	R	0

Table 4-38 : Counter 2 Data Register

Counter 2 Data Register will not load again while the latch is active. If a Latch Mode event occurs while Counter 2 Data Register Latch is active, the OVFL_EXT bit in Counter 2 Status Register will be set to indicate that data was lost.

To avoid data inconsistencies this register is developed for a long word (32 bit) read/write access. Byte or word accesses on this register are not supported and will fail.

4.3.6.4 Counter 2 Control Register CNTCONT_EXT (Offset 0x015C)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:15</td><td>-</td><td>Reserved
Write: don't care
Read: always reads as '0'</td><td>-</td><td>0</td></tr>
<tr><td>14:12</td><td>POL_EXT</td><td>Input Polarity
The Input Polarity Control can be used to adapt the counter inputs to the input source polarity.
<table>
<tr><th>POL</th><th>Input</th><th>Polarity</th></tr>
<tr><td>14</td><td>TTL I/O line 7</td><td>0 = high active, 1 = low active</td></tr>
<tr><td>13</td><td>TTL I/O line 6</td><td>0 = high active, 1 = low active</td></tr>
<tr><td>12</td><td>TTL I/O line 5</td><td>0 = high active, 1 = low active</td></tr>
</table></td><td>R/W</td><td>000</td></tr>
<tr><td>11</td><td>CIEN_EXT</td><td>Enable Control Mode Interrupt
0 = Control Mode Interrupt disabled
1 = Control Mode Interrupt enabled
An interrupt will be generated on a control mode event.
For pending interrupts and interrupt acknowledge see Counter 2 Status Register CNTSTAT_EXT.</td><td>R/W</td><td>0</td></tr>
<tr><td>10</td><td>MIEN_EXT</td><td>Enable Match Interrupt
0 = Match Interrupt disabled
1 = Match Interrupt enabled
An interrupt will be generated when the counter value matches Counter 2 Compare Register CNTCMP_EXT.
For pending interrupts and interrupt acknowledge see Counter 2 Status Register CNTSTAT_EXT.</td><td>R/W</td><td>0</td></tr>
<tr><td>9:7</td><td>ZCM_EXT</td><td>Control Mode
The Control Mode determines how the counter interprets the Control Input (I/O line 7).
<table>
<tr><th>ZCM</th><th>Control Mode</th></tr>
<tr><td>000</td><td>No Control Mode</td></tr>
<tr><td>001</td><td>Load Mode</td></tr>
<tr><td>010</td><td>Latch Mode</td></tr>
<tr><td>011</td><td>Gate Mode</td></tr>
<tr><td>100</td><td>Reset Mode</td></tr>
</table>
See chapter ‘Control Modes’ for details.</td><td>R/W</td><td>000</td></tr>
<tr><td>6:5</td><td>SCM_EXT</td><td>Count Mode
The Count Mode determines the behavior of the counter.
<table>
<tr><th>SCM</th><th>Count Mode</th></tr>
<tr><td>00</td><td>Cycling Counter</td></tr>
<tr><td>01</td><td>Divide-by-N</td></tr>
<tr><td>10</td><td>Single Cycle</td></tr>
</table>
See chapter ‘Count Modes’ for details.</td><td>R/W</td><td>00</td></tr>
<tr><td>4:3</td><td>CLKDIV_EXT</td><td>Internal Clock Prescaler
<table>
<tr><th>CLKDIV</th><th>Prescaler</th><th>Clock frequency</th></tr>
<tr><td>00</td><td>1x</td><td>40 MHz</td></tr>
<tr><td>01</td><td>2x</td><td>20 MHz</td></tr>
<tr><td>10</td><td>4x</td><td>10 MHz</td></tr>
<tr><td>11</td><td>8x</td><td>5 MHz</td></tr>
</table></td><td>R/W</td><td>00</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>2:0</td><td>INPUT_EXT</td><td>Input Mode
The Input Mode determines the input source for the counter and how the counter interprets these input signals. The quadrature mode can be used with a 1x, 2x, or 4x resolution multiplier.
<table>
<tr><th>INPUT</th><th>Input Mode</th><th>Input Source</th></tr>
<tr><td>000</td><td>Counter disabled</td><td>-</td></tr>
<tr><td>001</td><td>Timer Mode Up</td><td>Internal Clock Prescaler</td></tr>
<tr><td>010</td><td>Timer Mode Down</td><td>Internal Clock Prescaler</td></tr>
<tr><td>011</td><td>Direction Count</td><td>I/O line 5 & 6</td></tr>
<tr><td>100</td><td>Up/Down Count</td><td>I/O line 5 & 6</td></tr>
<tr><td>101</td><td>Quadrature Count 1x</td><td>I/O line 5 & 6</td></tr>
<tr><td>110</td><td>Quadrature Count 2x</td><td>I/O line 5 & 6</td></tr>
<tr><td>111</td><td>Quadrature Count 4x</td><td>I/O line 5 & 6</td></tr>
</table>
See chapter ‘Input Modes’ for details.</td><td>R/W</td><td>000</td></tr>
</table>

Table 4-39 : Counter 2 Control Register

Interrupts are generated only if the Master Interrupt Enable (MIE) is enabled in the Interrupt Control Register ICR.

4.3.6.5 Counter 2 Status Register CNTSTAT_EXT (Offset 0x0160)

Bit	Symbol	Description	Access	Reset Value
31:10	-	Reserved Read: always reads as '0'	R	0
9	CIRQ_EXT	Pending Control Mode Interrupts (Read), Interrupt acknowledge (Write) On a read-access this bit shows a pending Control Mode Interrupt. Pending interrupts are marked with a '1'. An interrupt is acknowledged by writing a '1' to this bit.	R/C	0
8	MIRQ_EXT	Pending Match Interrupts (Read), Interrupt acknowledge (Write) On a read-access this bit shows a pending Match Interrupt. Pending interrupts are marked with a '1'. An interrupt is acknowledged when the MAT_EXT bit is cleared.	R	0
7	SGL_EXT	Single Cycle active In Single Cycle counting mode this bit is set to ‘1’ if the counter is enabled.	R	0
6	OVFL_EXT	Counter 2 Data Register Latch Overflow If a Latch Mode event occurs while Counter 2 Data Register Latch is active, this bit will be set to indicate that data was lost. This bit must be reset by writing a '1' to this bit.	R/C	0
5	CDLT_EXT	Counter 2 Data Register Latch This bit is set to '1', when Counter 2 Data Register is latched due to a 'Latch on Control. This bit is cleared after a read access to the Output Register or by writing a '1' to this bit.	R/C	0
4	DIR_EXT	Count Direction This bit indicates the direction, the counter is counting to. '1' indicates up, '0' indicates down. In the 'Up/Down Count' mode this bit indicates the direction at the last count. In the 'Direction Count' mode this bit corresponds to the Y-input.	R	0
3	SGN_EXT	Sign The Sign bit is set to '1' when the counter overflows, and set to '0' when the counter underflows. After reset or power-up this bit should be considered as "don't care" until the first Carry or Borrow occurred.	R	0
2	MAT_EXT	Match This bit is set to '1' when the counter value matches the value of Counter 2 Compare Register. This bit must be reset by writing a '1' to this bit.	R/C	0
1	CRY_EXT	Carry This bit is set to '1' when the counter changes from 0xFFFFFFFF to 0x00000000. This bit must be reset by writing a '1' to this bit.	R/C	0
0	BOR_EXT	Borrow This bit is set to '1' when the counter changes from 0x00000000 to 0xFFFFFFFF. This bit must be reset by writing a '1' to this bit.	R/C	0

Table 4-40 : Counter 2 Status Register

4.3.6.6 Counter 2 Command Register CNTCOM_EXT (Offset 0x0164)

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved Write: don't care	-	-
1	LCNT_EXT	Load Counter Write '1' to load the counter with the value of Counter 2 Preload Register CNTPRL_EXT. This bit is cleared immediately after a write access.	W	0
0	RCNT_EXT	Reset Counter Write '1' to reset the counter. This bit is cleared immediately after a write access.	W	0

Table 4-41 : Counter 2 Command Register

4.3.7 Board Status Register

4.3.7.1 Temperature Register BOARD_TEMP (Offset 0x01F4)

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved	-	-
15:0	TEMP	Board Temperature Temperature (°C) = TEMP * 1/256 The temperature is provided as an signed value and continuously measured via the on PCT2075 on board device.	R	-

Table 4-42 : Temperature Register

4.3.7.2 Scratchpad Register BOARD_SCRATCH (Offset 0x01F8)

Bit	Symbol	Description	Access	Reset Value
31:0	SCRATCH	Scratchpad Register Can be used to test read and write operations	R/W	x"87654321"

Table 4-43 : Scratchpad Register

4.3.7.3 Firmware Identification Register BOARD_FIRM (Offset 0x01FC)

Bit	Symbol	Description	Access	Reset Value
31:24	FW_MAJ	Firmware Major Version	R	x"02"
23:16	FW_MIN	Firmware Minor Version	R	x"01"
15:8	FW_REV	Firmware Revision	R	-
7:0	FW_BLD	Firmware Build Count	R	-

Table 3-44 : Firmware Identification Register

4.4 ADC Sequencer Data RAM

PCI Base Address:	PCI Base Address 3 (Offset 0x1C in PCI Configuration Space).

The ADC Sequencer Data RAM is a 32 x 16 bit wide RAM storing the converted data values.

Each channel has its own ADC Data location.

The ADC Sequencer Data RAM is updated after every full sequencer cycle. Only the channels enabled in the ADC Sequencer Instruction RAM are updated.

Offset to PCI Base Address 3	Description	Size (Bit)
0x00	Channel 1 ADC Sequencer Data	16
0x02	Channel 2 ADC Sequencer Data	16
…	…	…
0x3C	Channel 31 ADC Sequencer Data	16
0x3E	Channel 32 ADC Sequencer Data	16

Table 4-45 : ADC Sequencer Data RAM Space Address Map

4.5 ADC/DAC Correction Data ROM

PCI Base Address:	PCI Base Address 4 (Offset 0x20 in PCI Configuration Space).

The correction data values are determined during the factory acceptance test, stored in an on-board EEPROM and made available in this write-protected space.

There is one Offset Error value and one Gain Error value (common for all 32 channels) for each ADC gain. For the DAC function there is an Offset Error value and a Gain Error value for each DAC channel.

See the Programming Hints chapter for data correction formulas.

The correction data space is write-protected.

The correction data is available approx. 500 µs after reset.

Offset to PCI Base Address 4	Description	Size (Bit)
0x00	ADC $Offset_{ERROR}$ Gain 1	16
0x02	ADC $Gain_{ERROR}$ Gain 1	16
0x04	ADC $Offset_{ERROR}$ Gain 2	16
0x06	ADC $Gain_{ERROR}$ Gain 2	16
0x08	ADC $Offset_{ERROR}$ Gain 4	16
0x0A	ADC $Gain_{ERROR}$ Gain 4	16
0x0C	ADC $Offset_{ERROR}$ Gain 8	16
0x0E	ADC $Gain_{ERROR}$ Gain 8	16
0x10	DAC Channel 1 $Offset_{ERROR}$	16
0x12	DAC Channel 1 $Gain_{ERROR}$	16
0x14	DAC Channel 2 $Offset_{ERROR}$	16

0x16	DAC Channel 2 $Gain_{ERROR}$	16
0x18	DAC Channel 3 $Offset_{ERROR}$	16
0x1A	DAC Channel 3 $Gain_{ERROR}$	16
0x1C	DAC Channel 4 $Offset_{ERROR}$	16
0x1E	DAC Channel 4 $Gain_{ERROR}$	16
0x20	DAC Channel 5 $Offset_{ERROR}$	16
0x22	DAC Channel 5 $Gain_{ERROR}$	16
0x24	DAC Channel 6 $Offset_{ERROR}$	16
0x26	DAC Channel 6 $Gain_{ERROR}$	16
0x28	DAC Channel 7 $Offset_{ERROR}$	16
0x2A	DAC Channel 7 $Gain_{ERROR}$	16
0x2C	DAC Channel 8 $Offset_{ERROR}$	16
0x2E	DAC Channel 8 $Gain_{ERROR}$	16

Table 4-46 : ADC/DAC Correction Data ROM Address Map

5 Configuration Hints

5.1 Local Software Reset

A Local Software Reset signal may be used to reset the on board local logic.

The local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the Miscellaneous Control Register CNTRL (offset 0x50) in the PCI Controller Register Space.

CNTRL[30] PCI Adapter Software Reset:

Value of 1 issues a reset to the local logic. The local logic remains in this reset condition until the PCI Host clears the bit. The contents of the PCI Controller Configuration Registers are not reset.

6 Programming Hints

6.1 Data Correction

There are two errors which affect the DC accuracy of the ADC and the DACs.

- Offset Error:

  ADC: The data value when converting with the input connected to its own ground in single-ended mode, or with shorted inputs in differential mode. This error is corrected by subtracting the known error from the readings.

  DAC: The data value that is required to get a zero voltage output signal. This error is corrected by subtracting the known error from the data value.

- Gain Error:

  ADC: The difference between the ideal gain and the actual gain of the programmable gain amplifier and the ADC. It is corrected by multiplying the reading with a correction factor.

  DAC: The difference between the ideal gain and the actual gain of the DAC. It is corrected by multiplying the data value with a correction factor.

The data correction values are obtained during the factory acceptance test and are stored in the Correction Data ROM.

6.1.1 ADC Correction Formula

Please use the total 16 bit data register value for the ADC correction formula.

The basic formula for correcting any ADC reading for the TPMC851 (bipolar input voltage range) is:

$$Value = Reading \cdot \left(1 - \frac{Gain_{corr}}{131072}\right) - \frac{Offset_{corr}}{4}$$

Value is the corrected result.

Reading is the data read from the ADC Data Register.

$Gain_{corr}$ and $Offset_{corr}$ are the ADC correction factors from the Correction Data ROM stored for each gain factor and are the same for all channel 1-32.

The correction values are stored as two's complement 16 bit values in the range -32768 to 32767. For higher accuracy they are scaled to ¼ LSB.

Floating point arithmetic or scaled integer arithmetic is necessary to avoid rounding error while computing above formula.

6.1.2 DAC Correction Formula

The basic formula for correcting any DAC value is:

$$Data = Value \cdot \left(1 - \frac{Gain_{corr}}{131072}\right) - \frac{Offset_{corr}}{4}$$

Value is the desired DAC value.

Data is the corrected DAC value that must be sending to the DAC.

$Gain_{corr}$ and $Offset_{corr}$ are the DAC correction values from the Correction Data ROM. They are stored separately for each of the 8 DAC channels.

The correction values are stored as two's complement byte wide values in the range from –32768 to +32767. For higher accuracy they are scaled to ¼ LSB.

Floating point arithmetic or scaled integer arithmetic must be used to avoid rounding errors in computing above formula.

6.2 ADC Operating Modes

The ADC part of the TPMC851 can operate in two modes: the Manual Mode, with little or none support through automation, and the Sequencer Mode, with large support through automation.

- Manual Mode

  In this mode, the converter operation relies on the user. The channel and gain are set by the user, and the user has large influence on the converter operation.

  Use this mode to convert specific channels and to control conversion timing or to read a channel repeatedly without the need to await the settling time.

- Sequencer Mode

  In this mode almost everything is automated and the converter operation is transparent to the user.

  Use this mode to convert all channels at specific time intervals, or to always have current data available.

6.2.1 Manual Mode

The Manual Mode is useful if direct control of converter operation is needed. Setup the desired channel and gain in the ADCCONT register. If the "Automatic Settling Time Control" is deactivated, the user has to wait until the ADC_SETTL flag reads '0'. Then the conversion can be started with a write access to the ADC Conversion Start Register ADCCONV. If the Automatic Settling Time Control is activated, the conversion starts automatically after the settling time has elapsed.

It is possible to select the next channel and/or gain in the ADCCONT register immediately after the write to the ADC Conversion Start Register ADCCONV. The conversion and the settling time will then proceed simultaneously.

The conversion data is available in the ADCDATA register when the ADC_BUSY flag in the ADCSTAT register reads as '0'.

If interrupts are enabled, two interrupts will be generated: the first interrupt is generated when the settling time has elapsed (and the Automatic Settling Time Control is deactivated); the second interrupt is generated when the conversion has finished. Using the interrupts exempts from polling the ADC_SETTL and ADC_BUSY flags.

Without Automatic Settling Time Control:

→ Setup the conversion in the ADC Control Register ADCCONT

→ Poll for SETTL_BUSY flag

→ After settling time has elapsed, write to the ADC Conversion Start Register ADCCONV to start conversion

→ Poll for ADC_BUSY flag

→ After conversion time has elapsed, read conversion data in the ADC Data Register ADCDATA

With Automatic Settling Time Control:

→ Setup the conversion in the ADC Control Register ADCCONT

→ Poll for SETTL_BUSY flag

→ Poll for ADC_BUSY flag

→ After conversion time has elapsed, read conversion data in the ADC Data Register ADCDATA

6.2.2 Sequencer Mode

The Sequencer Mode is very useful for periodic measurements or to always provide actual conversion data. The sequencer converts all enabled ADC channels and stores the results in the Sequencer Data RAM. After a programmable time the sequencer repeats the sequence.

To use the sequencer, all channels must be configured for the sequence in the Sequencer Instruction RAM. In the Sequencer Instruction RAM the channels are enabled for the sequence, and the gain and the mode (single-ended or differential) are selected.

Once the sequencer is started, all enabled channels are converted and the results are stored in the Sequencer Data RAM. When the last sequencer instruction has been completed, the Data Available Flag DATA_AV in the Sequencer Status Register (ADCSEQSTAT) is set to '1' and, if enabled, an interrupt request will be asserted. The user can now read the ADC data from the Sequencer Data RAM (note: only the enabled channels are updated; Channels not enabled in the Sequencer Instruction RAM are not updated and may contain invalid data from former conversions). After that, the DATA_AV flag must be cleared by writing a '1' to the Sequencer Status Register ADCSEQSTAT bit 0.

The repeat frequency of the sequencer can be programmed in the Sequencer Timer Register. The Sequencer Timer is programmable from 100µs to 6.5535s in steps of 100µs. Whenever the timer reaches the programmed value, the sequencer starts a new sequence.

A special function is the Sequencer Continuous Mode. It is activated if the Sequencer Timer Register is set to 0x0000. In this mode the sequencer immediately starts a new sequence when the actual sequence has been completed. If the sequencer is in Sequencer Continuous Mode, the user can read valid data from the Sequencer Data RAM at any time. The Sequencer Data RAM locations of the enabled ADC channels are updated with every sequence.

If the Sequencer Continuous Mode is active, the Timer Error Flag (TIMER_ERROR) and the Data Overflow Error Flag (DATA_OVERFLOW_ERROR) are not active and will read as ‘0’. Clearing the Data Available Flag DATA_AV is not necessary in the Sequencer Continuous Mode (it will not produce an interrupt), but it may be useful in order to monitor the completion of the sequences.

The sequencer may also be triggered by an external signal instead of the timer. In this case the Timer Error Flag (TIMER_ERROR) is not active. A new external trigger is accepted only after a sequence has completed. An external trigger while the sequencer runs is ignored.

The update rate depends on the number of enabled channels:

Update Rate = 16µs · number of enabled channels

6.2.2.1 Sequencer Errors

If the sequencer detects an error, it will stop after the last instruction and sets the corresponding error flag in the Sequencer Status Register SEQSTAT.

Error	Description	Sequencer Action	User Action
Data Overflow Error	Error occurs if the sequencer has new data to store but the user has not yet acknowledged that the data from the previous sequence has been read out. (not in Sequencer Continuous Mode)	Sequencer stops after the last instruction is done. Data Overflow Error Flag is set. If enabled, an interrupt request will be asserted.	Write a '1' to the Sequencer Status Register bit 1. Make sure the Sequencer Data is read and acknowledged within the programmed Sequence Time. Start Sequencer again.
Timer Error	Error occurs if the programmed Sequencer Time is shorter than the sequence itself. (not in Sequencer Continuous Mode)	Sequencer stops after the last instruction is done. Timer Error Flag is set. If enabled, an interrupt request will be asserted.	Write a '1' to the Sequencer Status Register bit 2. Program a larger Sequence Time. Start Sequencer again.
Instruction RAM Error	Error occurs if the no channel is enabled for the sequence (bit 1 of Sequencer Instruction RAM byte) and the Sequencer is started.	Sequencer stops after the last instruction is done. Instruction RAM Error Flag is set. If it is enabled, an interrupt request will be asserted.	Write a '1' to the Sequencer Status Register bit 3. Correct the Sequencer Instruction RAM setting. Start Sequencer again.

Table 6-1 : Sequencer Errors

If the Sequence Timer Register is set to 0x0000 (Sequencer Continuous Mode) the sequencer ignores the data overflow. The Data Overflow Error Flag is always read as '0' in this mode.

6.2.3 Application Examples

The following examples all use interrupts. The use of interrupts can be replaced by polling the according status flags in the ADC Status Register or the Sequencer Status Register.

6.2.3.1 Fastest Conversion of an arbitrary Single Channel

→ Program the desired channel and gain in the ADC Control Register ADCCONT. Activate the Automatic Settling Time Control (ASTC = '1') and the IRQ after Conversion (IRQC = '1')

→ The channel is now converted without any further user action. After completion of the conversion an interrupt is issued which signals that the conversion data is available in the ADCDATA Register

→ Acknowledge the Interrupt in the ADC Status Register ADCSTAT (ADC_READY = '1') and read ADCDATA

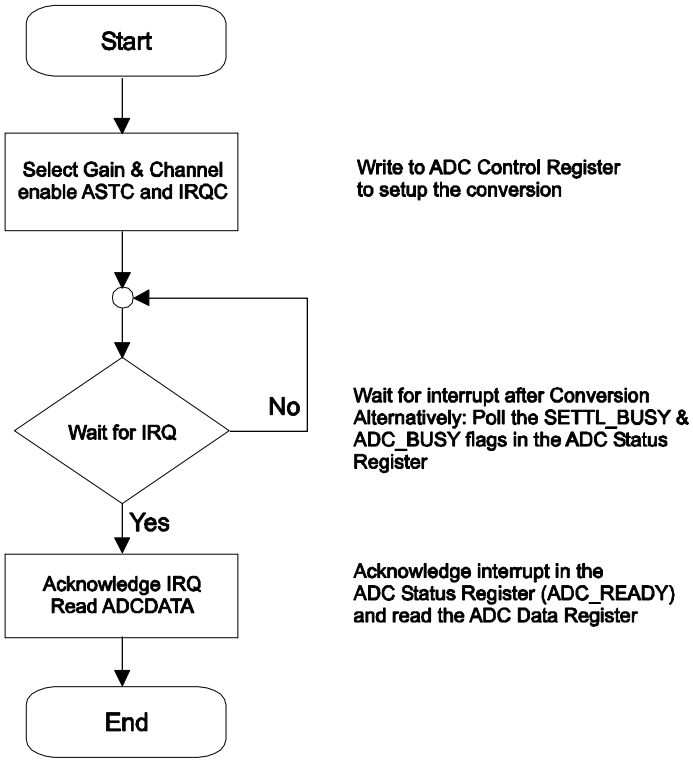

Figure 6-1 : Flow: Fastest conversion of an arbitrary single channel

Conversion time is approx. 17.25µs.

6.2.3.2 Fastest Conversion of a specific Single Channel

→ Program the ADC Control Register with desired channel and gain and activate the IRQ after Settling Time (IRQS = '1') and the IRQ after Conversion (IRQC = '1')

→ When the IRQ after Settling Time is issued, the channel is ready for conversion. Write to the ADC Conversion Start Register ADCCONV and acknowledge the Interrupt in the ADC Status Register ADCSTAT (SETTL_IRQ = '1')

→ After completion of the conversion an IRQ after Conversion is issued which signals that the conversion data is available in the ADCDATA Register

→ Write again to the ADC Conversion Start Register ADCCONV to start the next conversion of this channel, acknowledge the Interrupt in the ADC Status Register ADCSTAT (ADC_IRQ = '1') and read ADCDATA.

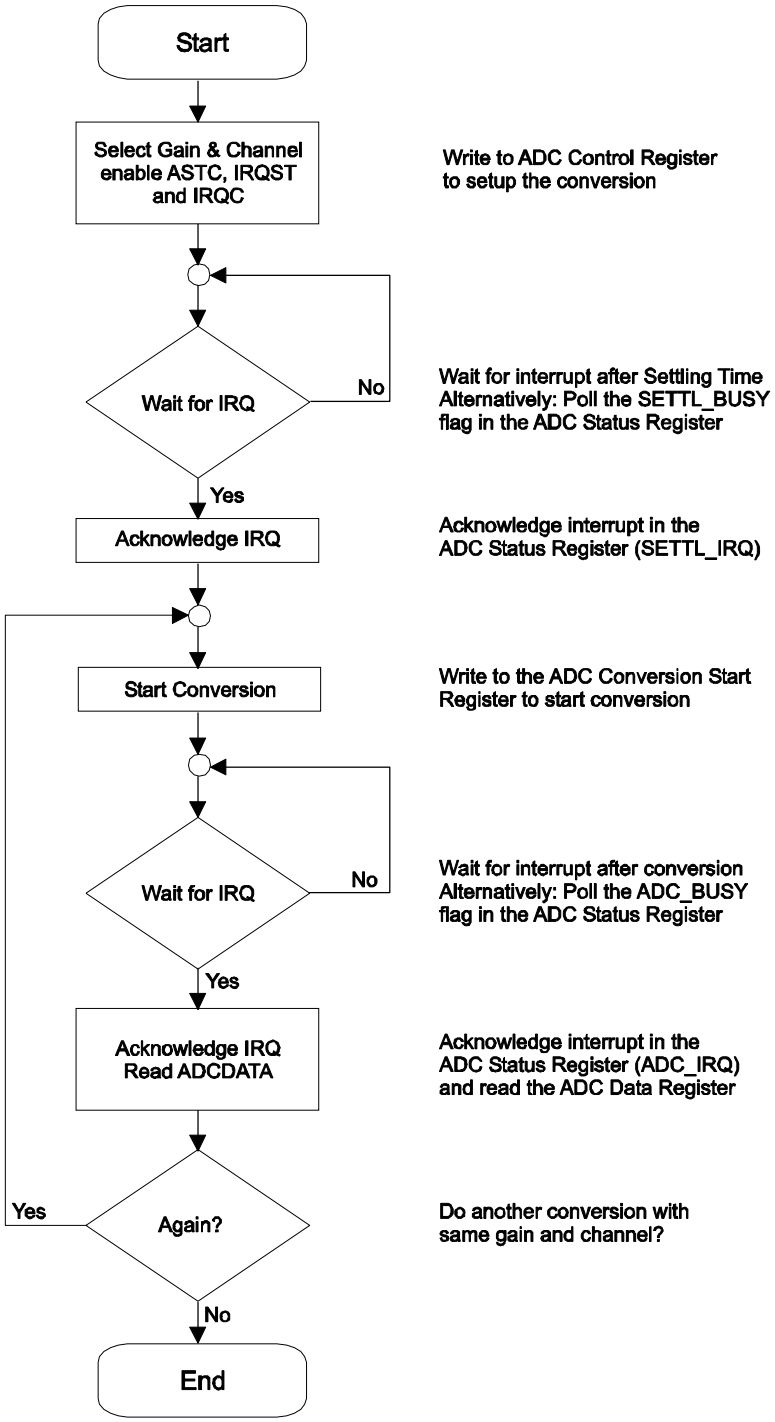

Figure 6-2 : Flow: Fastest conversion of a specific single channel

Conversion time is approx 1.25µs, as long as neither the channel nor the gain is changed (ADC throughput rate up to 250ksps).

6.2.3.3 Periodic Conversion of multiple Channels

- → Activate the channels to be converted and program the gain in the Sequencer Instruction RAM
- → Set the sequencer period in the ADC Sequencer Timer Register ADCSEQTIMER
- → Enable the Sequencer Interrupt SEQ_INT_ENA and start the Sequencer in the Sequencer Control Register ADCSEQCONT
- → After completion of the sequence a Sequencer Interrupt is issued which signals that the conversion data is available in the Sequencer Data RAM
- → Acknowledge the Interrupt and clear the DATA_AV flag in the ADC Sequencer Status Register ADCSEQSTAT (SEQ_IRQ = '1') and read the Sequencer Data RAM

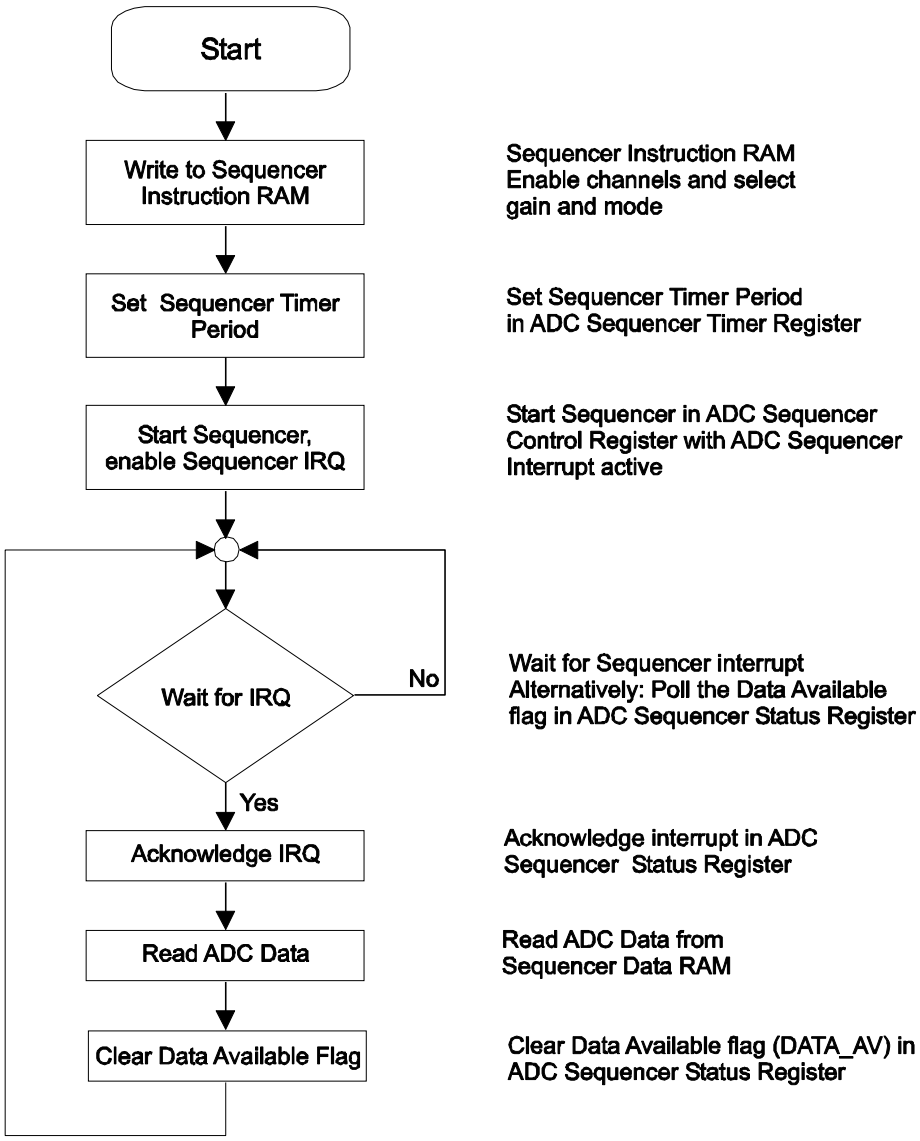

Figure 6-3 : Flow: Periodic conversion of multiple channels

6.2.3.4 Continuous Conversion of multiple Channels

- → Activate the channels to be converted and program the gain and mode of these channels in the Sequencer Instruction RAM
- → Set the Sequencer Timer Register ADCSEQTIMER to 0x0000
- → Start the Sequencer in the Sequencer Control Register ADCSEQCONT
- → Read the data from the Sequencer Data RAM as needed.

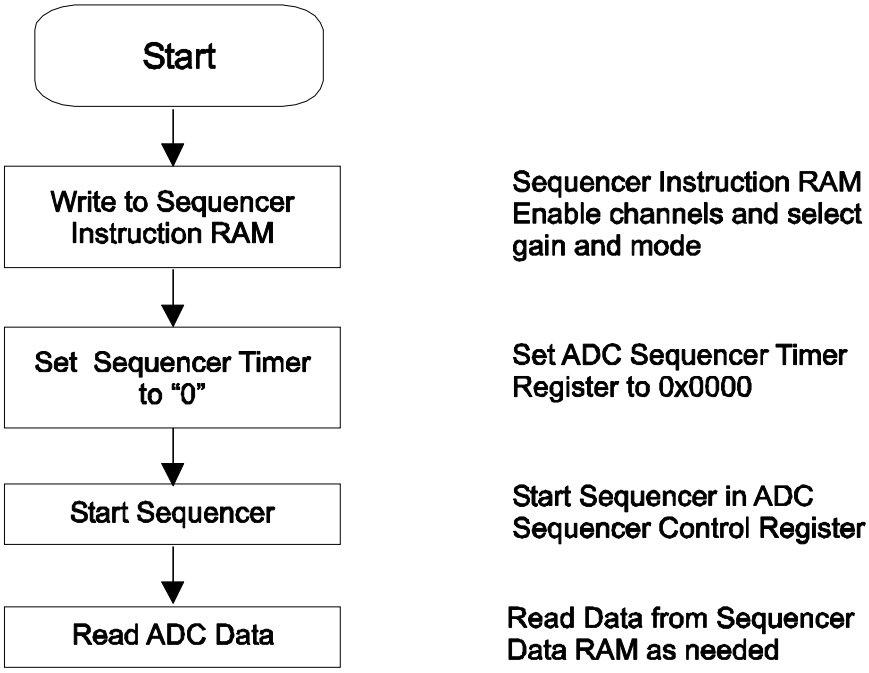

Figure 6-4 : Flow: Continuous conversion of multiple channels

6.3 DAC Operating Modes

The DAC part of the TPMC851 can operate in two modes – Immediate Update or Simultaneous Update. These modes are configured with the Load Mode Select (LOADSEL) bits in the DAC Control Register DACCONT.

LOADSEL[1:0]	Load Mode
Immediate Update	
00	Immediate Update: The DAC outputs are updated immediately on a write access to a DAC Data Register
Simultaneous Update	
01	Simultaneous Update: All DAC outputs are updated simultaneously when LOADDAC is set to '1'
10	Sequencer Update: All DAC outputs are updated simultaneously when the DAC Sequencer Timer reaches zero
11	Trigger Update: All DAC outputs are updated simultaneously by an external trigger (Dig I/O Line 1)

Table 6-2 : DAC Load Modes

6.3.1 Immediate Update

The DACs are updated immediately on a write access to a DAC Data Register. Use this mode if single channels need to be updated on an irregular base.

6.3.2 Simultaneous Update

Write accesses to the DAC Data Registers don't immediately update the DACs. Instead this data is buffered until a trigger event. This trigger event simultaneously updates all DACs with the buffered data. The Simultaneous Update Mode divides into three sub modes. These modes vary in the source for the trigger event:

- Simultaneous Update: The DACs are updated simultaneously when LOADDAC in the DAC Control Register DACCONT is set to '1'. Use this mode if all channels need to be updated on an irregular base.
- Sequencer Update: All DAC outputs are updated simultaneously when the DAC Sequencer Timer reaches zero. Use this mode if all channels need to be updated on a regular base.
- Trigger Update: All DAC outputs are updated simultaneously by an external trigger (Dig I/O Line 1). Use this mode if all channels need to be updated on an external event.

Before a simultaneous update all DACs should be loaded with new data via the DAC Data Registers. If a channel was not loaded with new data, it will use the old data previously buffered.

Allow the DAC outputs to settle for approx. 10µs before performing a new DAC update.

6.4 Digital TTL I/O

Note that some digital inputs are internally used in the other parts of the TPMC851:

TTL I/O line 0 as ADC sequencer trigger input/output

TTL I/O line 1 as DAC sequencer trigger input/output

TTL I/O lines 2,3,5 and 6 as inputs for the counters

TTL I/O lines 4 and 7 as control inputs for the counters

Normally the usage of these digital I/O lines is not subject to any restrictions, as long as they are used as inputs (i.e. as trigger for a sequencer). Exceptions are I/O lines 0 and 1, these can also be used as sequencer trigger output.

If ADC_OUT in the Line Direction Register LINEDIR is set to '1', the trigger signal for the ADC sequencer is available for external use on Dig I/O Line 0.

If DAC_OUT in the Line Direction Register LINEDIR is set to '1', the trigger signal for the DAC sequencer is available for external use on Dig I/O Line 1.

In this case the settings in the Line Direction Register for these I/O lines (LINEDIR0 resp. LINEDIR1) are overridden and they are always used as output. Writes in the Line Output Register to these I/O lines (LINEOUT0 resp. LINEOUT1) have no effect.

Avoid to use this configuration while the sequencer is set to wait for an external trigger (ADC: SEQ_TRIG = 1; DAC: LOAD_SEL = 11). This will cause the sequencer to lock.

If it is required to use the I/O line as sequencer trigger input and output at the same time, this can be achieved with following solution:

→ Configure the sequencer to wait for an external trigger (ADC: SEQ_TRIG = 1; DAC: LOAD_SEL = 11)

→ Configure the I/O Line as output (ADC: LINEDIR0 = 1; DAC: LINEDIR1 = 1)

→ Trigger the sequencer with a write to the Line Output Register (ADC: LINEOUT0 = 1; DAC: LINEOUT1 = 1)

6.5 Counter Operating Modes

The general purpose counters of the TPMC851 offer 4 Input Modes, 3 Count Modes and 4 Control Modes.

6.5.1 Input Modes

The Input Mode determines the input source for the counters and how the counters interpret these input signals:

Input Mode	I/O Line 2 I/O Line 5	I/O Line 3 I/O Line 6	I/O Line 4 I/O Line 7
Timer Mode	-	-	Available for Control Modes
Direction Count	Count	Count direction (up/down)	
Up/Down Count	Count UP	Count DOWN	
Quadrature Count	Quadrature X	Quadrature Y	

Table 6-3 : Input Modes

Changing the input mode does not affect the counters reading. If no input mode is selected, the counters are disabled.

6.5.1.1 Timer Mode

In Timer Mode the counters are using an internal clock prescaler as input:

Bits	Prescaler	Clock frequency
00	1x	40 MHz
01	2x	20 MHz
10	4x	10 MHz
11	8x	5 MHz

Table 6-4 : Clock Prescaler

6.5.1.2 Direction Count

The counters act as up/down counters. Counting pulses are generated when a transition from low to high of I/O Lines 2/5 is detected. I/O Lines 3/6 determine the count direction. I/O Line 3/6 = '1' is up, I/O Line 3/6 = '0' is down.

I/O Line 3 I/O Line 6	Count Direction
0	Down
1	Up

Table 6-5 : Count Direction

6.5.1.3 Up/Down Count

The counters act as up/down counters. Counting pulses are generated when a transition from low to high of either the I/O Lines 2/5 or the I/O Lines 3/6 is detected. The I/O Lines 2/5 count up, the I/O Lines 3/6 count down. Simultaneous transitions on both I/O lines do not generate a counting pulse.

6.5.1.4 Quadrature Count

The counters act as quadrature counters. The quadrature inputs can be interpreted as 1x, 2x or 4x counting. 1x lets the counters count once for each full cycle of the quadrature inputs, 2x lets the counters count once for each half cycle of the quadrature inputs and 4x lets the counters count once for each quarter cycle of the quadrature inputs. The count direction (increase or decrease) is determined by the relative phase of the Quadrature X- and Quadrature Y-signals.

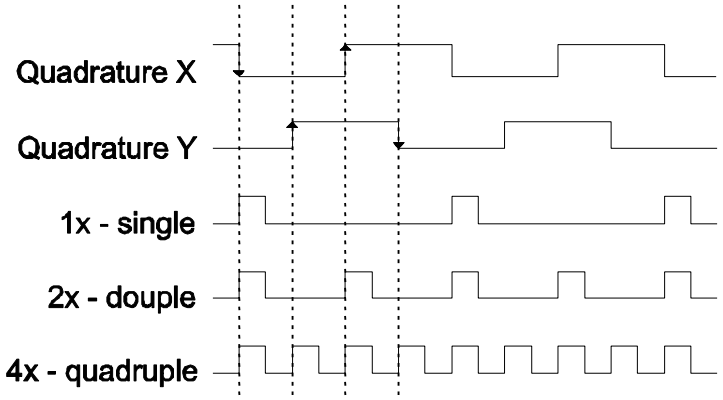

Figure 6-5 : Quadrature Signals

6.5.2 Count Modes

In normal operation, the counters are cyclic counters. Additional two Count Modes are available. The Count Modes are available for every Input Mode.

6.5.2.1 Divide-by-N

The counters are enabled in their respective Channel Control Register and will run until disabled. The counters are loaded with the content of the respective preload register every time the counters create a borrow or a carry. This mode assumes that the counters count in one direction only.

6.5.2.2 Single Cycle

The counters are enabled in their respective Channel Control Register and will start on a manual preload or reset in the respective Channel Command Register or on a control mode event in load or reset mode.

The counters stop when they create a borrow or a carry.

6.5.3 Control Modes

The Control Mode determines how I/O Lines 4/7 are interpreted. A control mode event generates interrupts, if the Control Mode Interrupt is enabled in the Counters Control Registers.

With the exception of the Gate Mode, all modes react on a level change on I/O Lines 4/7. Note that if the digital debounce filter is applied, a change in the input level is only detected when the input line is stable for duration greater than the programmed debounce duration.

The following table gives an overview of the control mode events.

Input Control Mode	Polarity	
	high active (CNTCONT[14] = 0) (CNTCONT_EXT[14] = 0)	**low active (CNTCONT[14] = 1) (CNTCONT_EXT[14] = 1)**
No Control Mode	-	-
Load Mode	Rising edge	Falling edge
Latch Mode	Rising edge	Falling edge
Gate Mode	High level	Low Level
Reset Mode	Rising edge	Falling edge

Table 6-6 : Input Control Mode events

6.5.3.1 No Control Mode

In this mode I/O Lines 4/7 are ignored.

6.5.3.2 Load Mode

An event on I/O Lines 4/7 loads the counters with the content of their respective Counter Preload Register.

If the 'Single Cycle' mode is active, the event on I/O Lines 4/7 starts the counters.

The counters can also be preloaded by writing '1' to the 'Load Counter' (LCNT/LCNT_EXT) bit in the respective Channel Command Register.

6.5.3.3 Latch Mode

An event on I/O Lines 4/7 latches the actual counter value in their respective Counter Data Register. It will remain latched until the Counter Data Registers are read or the latch is released with the CDLT/CDLT_EXT bit in the Counters Status Registers.

6.5.3.4 Gate Mode

The I/O Lines 4/7 enable or disable counting.

I/O Line 4 I/O Line 7	Counter
0	Disabled
1	Enabled

Table 6-7 : Gate Mode

In this mode an interrupt is generated (if enabled) if the gate is closed.

6.5.3.5 Reset Mode

An event on I/O Lines 4/7 resets the counters.

If the 'Single Cycle' mode is active, the event on I/O Lines 4/7 starts the counters.

The counters can also be reset by writing '1' to the Reset Counter (RCNT/RCNT_EXT) bit in the Channel Command Registers.

6.5.4 Configuration Examples

6.5.4.1 Watchdog Timer

The watchdog timer counts down from a programmed value until it reaches 0. The counters must be reloaded on a regular base either internal via Counters Command Registers or external via I/O Line 4/7. Failure to cause a reload would generate a timeout and an interrupt.

Input Mode	Count Mode	Control Mode	Additional Configuration
Timer Mode Down	Single Cycle	Load Mode	Set CNTPRL/CNTPRL_EXT to watchdog time, CNTCMP/CNTCMP_EXT to zero, enable counter match IRQ

6.5.4.2 Event Counting

In this configuration, input pulses or events occurring at the input pin of the counters are counted up to a programmed count limit. Upon reaching the count limit, the counters outputs will generate an interrupt. To arm the counters for the next measurement, reset the counters in their Counter Command Registers.

Input Mode	Count Mode	Control Mode	Additional Configuration
U/D Count	Single Cycle	none	Set CNTCMP/CNTCMP_EXT to limit, enable counter match IRQ

6.5.4.3 Input Pulse Width Measurement

For pulse-width measurement, the pulse-width being measured serves as a clock gate for an up-counter. To arm the counters for a measurement, reset the counters in their Counter Command Registers. The measurement starts with the next rising edge and ends with the falling edge of the gate signal. An interrupt is generated upon completion of the pulse-width measurement. The up-counter uses the internal clock prescaler at the counter's clock pin. Use following formula to calculate the pulse-width:

Pulse Width = Counter Value / Clock Frequency

Input Mode	Count Mode	Control Mode	Additional Configuration
Timer Mode Up	Single Cycle	Gate Mode	Enable control mode IRQ

6.5.4.4 Mechanical System Positioning

If a mechanical system provides position switches, these can be used for various purposes:

Establish a known home

Input Mode	Count Mode	Control Mode	Additional Configuration
U/D Count	Cycle Counter	Reset Mode	Enable control mode IRQ

Establish a known reference position

Input Mode	Count Mode	Control Mode	Additional Configuration
U/D Count	Cycle Counter	Load Mode	Enable control mode IRQ

Capture a position

Input Mode	Count Mode	Control Mode	Additional Configuration
U/D Count	Cycle Counter	Latch Mode	Enable control mode IRQ

6.6 Interrupts

All Interrupts are requested at the LINT1 input of the PCI Target Chip.

Interrupts are generated only if the Master Interrupt Enable (MIE) is enabled in the Interrupt Control Register ICR.

6.6.1 Interrupt Sources

IRQ	IRQ Description	Enable IRQ	Acknowledge IRQ
IRQST	ADC settling time elapsed	ADC Control Register ADCCONT	ADC Status Register ADCSTAT
IRQC	ADC conversion finished	ADC Control Register ADCCONT	ADC Status Register ADCSTAT
SEQ IRQ	ADC sequencer interrupt	ADC Sequencer Control Register ADCSEQCONT	ADC Sequencer Status Register ADCSEQSTAT
DAC IRQ	DAC sequencer interrupt	DAC Control Register DACCONT	DAC Sequencer Status Register DACSEQSTAT
LINEIST	Digital I/O line IRQ	Line Interrupt Enable Register LINEIEN	Line Interrupt Status Register LINEIST
CIRQ	Counter control mode interrupt 1	Counter 1 Control Register CNTCONT	Counter 1 Status Register CNTSTAT
MIRQ	Counter match interrupt 1	Counter 1 Control Register CNTCONT	Counter 1 Status Register CNTSTAT
CIRQ_EXT	Counter control mode interrupt 2	Counter 2 Control Register CNTCONT_EXT	Counter 2 Status Register CNTSTAT_EXT
MIRQ_EXT	Counter match interrupt 2	Counter 2 Control Register CNTCONT_EXT	Counter 2 Status Register CNTSTAT_EXT

Table 6-8 : Interrupt sources

The Interrupt Control Register can give a quick overview which interrupt source caused an interrupt.

7 Installation

7.1 ADC Input Wiring

The TPMC851 provides 32 single-ended or 16 differential multiplexed analog inputs. The desired input channel and the mode (single-ended or differential) are selected by programming the input multiplexer.

A software programmable gain amplifier with gain settings of 1, 2, 4 and 8 allows a direct connection of a wide range of sensors and instrumentation. The maximum analog input voltage range is ±10V at a gain of 1.

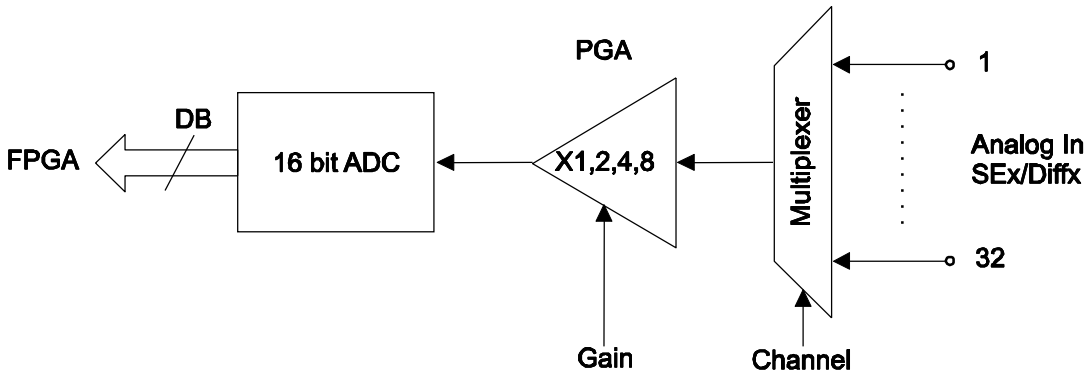

Figure 7-1 : ADC Input Wiring

Make sure that all unused analog input pins are tied to the GND signal level (or any other valid signal level within the analog input voltage range). This is required even if the unused channels are turned off by software.

If unused analog inputs are left floating, they could badly degrade the performance of the active channels.

7.2 DAC Output Wiring

The DAC is used to generate the ±10V analog output voltage. The operational amplifier is able to drive high capacitance loads and protects the DAC.

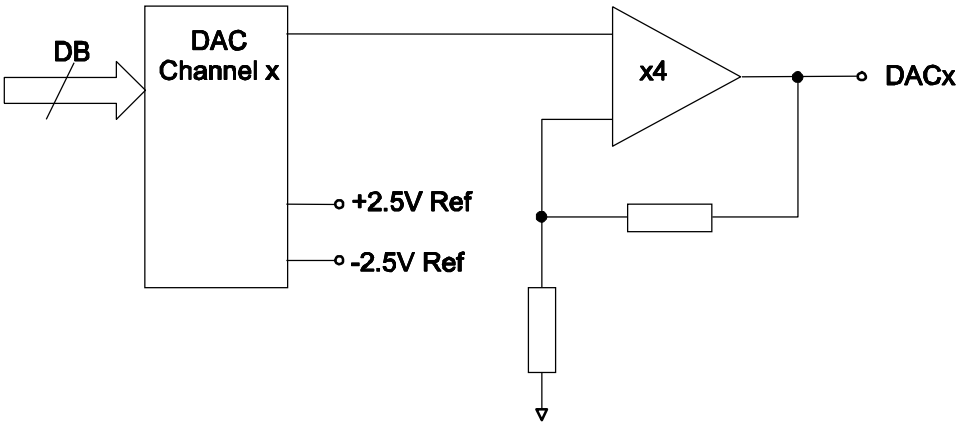

Figure 7-2 : DAC Output Wiring

7.3 TTL Digital I/O Interface

In total, 16 TTL I/O lines are available on the standard TPMC851. These I/O lines are utilized with an input and output buffer with a 4.7kΩ pull up resistor for the tri-state output function and an array for ESD protection. See the following figure for more information.

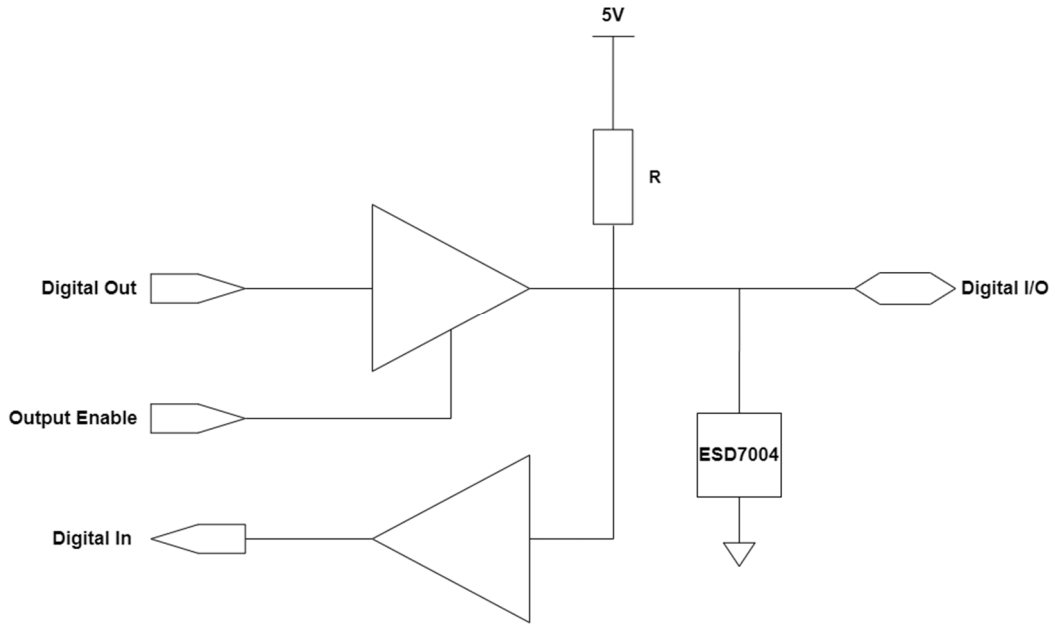

Figure 7-3 : TTL I/O Interface

While power-up and after reset all digital I/O lines are configured as inputs. Because of the pull-up resistor an unused (open) digital I/O line will be read as '1'. A digital I/O line configured as input will appear as a high state to the outside, as long it is not driven from the outside.

8 Pin Assignment – I/O Connector

Connector: HD68 SCSI-3 type female connector (AMP 787082-7)

Pin	Signal	
1	ADC SE 1	ADC Diff 1+
2	ADC SE 2	ADC Diff 2+
3	ADC SE 3	ADC Diff 3+
4	ADC SE 4	ADC Diff 4+
5	ADC SE 5	ADC Diff 5+
6	ADC SE 6	ADC Diff 6+
7	ADC SE 7	ADC Diff 7+
8	ADC SE 8	ADC Diff 8+
9	GND	
10	ADC SE 9	ADC Diff 9+
11	ADC SE 10	ADC Diff 10+
12	ADC SE 11	ADC Diff 11+
13	ADC SE 12	ADC Diff 12+
14	ADC SE 13	ADC Diff 13+
15	ADC SE 14	ADC Diff 14+
16	ADC SE 15	ADC Diff 15+
17	ADC SE 16	ADC Diff 16+
18	GND	
19	DAC 1 Output	
20	DAC 2 Output	
21	GND	
22	DAC 3 Output	
23	DAC 4 Output	
24	GND	
25	TTL I/O 0 (ADC Seq. Trg.)	
26	TTL I/O 1 (DAC Seq. Trg.)	
27	TTL I/O 2 (Counter 1 input)	
28	TTL I/O 3 (Counter 1 input)	
29	GND	
30	TTL I/O 4 (Counter 1 input)	
31	TTL I/O 5 (Counter 2 input)	
32	TTL I/O 6 (Counter 2 input)	
33	TTL I/O 7 (Counter 2 input)	
34	GND	

Pin	Signal	
35	ADC SE 17	ADC Diff 1-
36	ADC SE 18	ADC Diff 2-
37	ADC SE 19	ADC Diff 3-
38	ADC SE 20	ADC Diff 4-
39	ADC SE 21	ADC Diff 5-
40	ADC SE 22	ADC Diff 6-
41	ADC SE 23	ADC Diff 7-
42	ADC SE 24	ADC Diff 8-
43	GND	
44	ADC SE 25	ADC Diff 9-
45	ADC SE 26	ADC Diff 10-
46	ADC SE 27	ADC Diff 11-
47	ADC SE 28	ADC Diff 12-
48	ADC SE 29	ADC Diff 13-
49	ADC SE 30	ADC Diff 14-
50	ADC SE 31	ADC Diff 15-
51	ADC SE 32	ADC Diff 16-
52	GND	
53	DAC 5 Output	
54	DAC 6 Output	
55	GND	
56	DAC 7 Output	
57	DAC 8 Output	
58	GND	
59	TTL I/O 8	
60	TTL I/O 9	
61	TTL I/O 10	
62	TTL I/O 11	
63	GND	
64	TTL I/O 12	
65	TTL I/O 13	
66	TTL I/O 14	
67	TTL I/O 15	
68	GND	

Table 8-1 : Pin Assignment I/O Connector

9 Important Notes

9.1 Dummy Conversions after Power-up

After power-up the ADC's logic will be in a random state and may not perform correctly. This has two consequences:

1. The first conversion results are not valid and should be ignored.
2. The ADC starts in a mode that prevents a correct start of the sequencer.

Therefore, two dummy conversions are required after each power-up, whose results should be ignored.

Use the ADC Conversion Start Register (ADCCONV) Register to perform the dummy conversions.

If the sequencer is to be used, these two dummy conversions are absolutely necessary.

If a TEWS Technologies software drivers is used, these two dummy conversions are already included.

9.2 Open Multiplexer Inputs

Unused Multiplexer inputs can pick up stray signals which are injected into the device's substrate. This turns on spurious substrate devices which badly degrade the performance of the whole multiplexer device.

Make sure that all unused analog input pins are tied to the analog ground signal level (or any other valid signal level within the analog input voltage range). This is required even if the unused channels are turned off by software.