The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC700

32/16 Digital Outputs (24 V, 0.5 A)

Version 2.0

User Manual

Issue 2.0.0

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TPMC700-10R

32 digital outputs front panel I/O

TPMC700-11R

16 digital outputs front panel I/O

TPMC700-20R

32 digital outputs P14 I/O

TPMC700-21R

16 digital outputs P14 I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	September 1999
1.1	General Revision	April 2003
1.2	Description of optical isolation corrected	March 2004
1.3	Added differences of V1.1	June 2005
1.4	New address TEWS LLC	September 2006
1.1.0	New notation of HW Engineering Documentation Releases	November 2011
1.1.1	General Revision	August 2014
2.0.0	General Board Redesign to Version 2.0 due to component obsolescence. Fully backward compatible.	September 2024

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1 Product Description

The TPMC700 is a PMC compatible module which provide 32 (16) digital outputs with galvanic isolation via optocouplers. All outputs resist short-circuits and are protected against thermal overload. The output drivers are capable of driving 0.5 A continuous per channel as a high side switch. A hardware watchdog forces all outputs into safe state (disabled) in case of a trigger failure.

The TPMC700-1xR provides front panel I/O with a HD50 SCSI-2 type connector, the TPMC700-2xR provides P14 I/O.

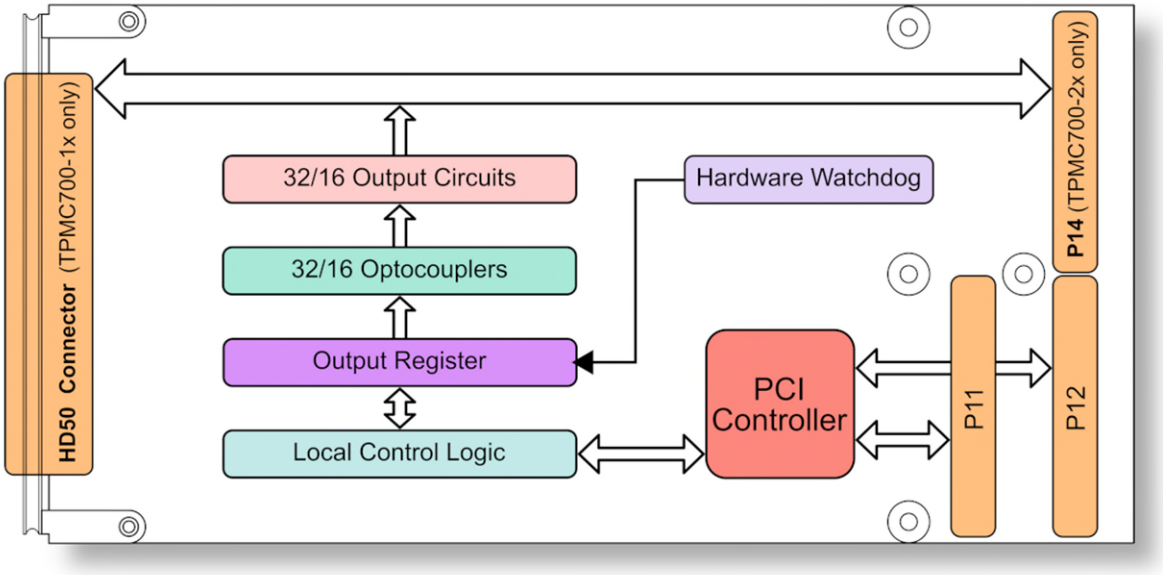

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size	
Electrical Interface	PCI Rev. 3.0 compatible 33 MHz / 32 bit PCI 3.3 V and 5 V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	TEWS PCI Interface FPGA	
I/O Interface		
Number of Outputs	TPMC700-10R/-20R: 32 digital outputs TPMC700-11R/-21R: 16 digital outputs	
Output Isolation	Optocouplers for galvanic isolation between system and output lines	
External Output Voltage	24 VDC typical, 6 VDC minimum, 48 VDC maximum	
Output Current	0.5 A typical (0.3 A for voltages over 32 V)	
Short Circuit Current	0.8 A typical	
Output Voltage Drop	1.1 V typical @ 0.5 A	
Output Protection	Overload, short circuit, GND and Vs open wire protection, thermal shutdown	
Watchdog	Maximum trigger distance = 120 ms	
I/O Connector	TPMC700-10R/-11R: HD50 SCSI-2 type connector (AMP 787395-5) or compatible TPMC700-20R/-21R: PMC P14 I/O (64 pin Mezzanine Connector)	
Physical Data		
Power Requirements	75 mA typical @ +5 VDC	
Temperature Range	Operating Storage	-25 °C to +85 °C -40 °C to +125 °C
MTBF	TPMC700-10R: 711 000 h TPMC700-11R: 858 000 h TPMC700-20R: 711 000 h TPMC700-21R: 858 000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	72 g	

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

This PMC module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done with appropriate care.

3.2 Ground for Isolated I/O

I/O Connector's isolated ground signals must be connected to external ground.

4 Addressing

4.1 PCI Configuration Space

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	02BC 1498
0x04	Status		Command		Y	0280 0000
0x08	Class Code			Revision ID	N	118000 00
0x0C	not supported	Header Type	not supported	not supported	Y[7:0]	00 00 00 00
0x10	Base Address Register 0 (BAR0)				Y	FFFFFF80
0x14	Base Address Register 1 (BAR1)				Y	FFFFFF81
0x18	Base Address Register 2 (BAR2)				Y	FFFFFFF0
0x1C	not supported				Y	00000000
0x20	not supported				Y	00000000
0x24	not supported				Y	00000000
0x28	not supported				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	s.b. 1498
0x30	not supported				Y	00000000
0x34	Reserved			Cap. Ptr.	N	000000 00
0x38	Reserved				N	00000000
0X3C	MAX_LAT	MIN_GNT	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00
0X40-0XFF	Reserved					00000000

Table 4-1 : PCI Configuration Space Header

Subsystem-ID Value (Offset 0x2C): TPMC700-10R 0x000A

TPMC700-11R 0x000B

TPMC700-20R 0x0014

TPMC700-21R 0x0015

4.2 PCI Address Space Overview

The local on board addressable regions are accessed from the PCI side by using the BAR2 Base Address.

PCI BAR	PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	0x10	MEM	128	32	Little	PCI Controller Register Space
1	0x14	I/O	128	32	Little	
2	0x18	MEM	16	32	Big	Local Register Space

Table 4-2 : PCI Address Space Overview

4.3 PCI Controller Register Space

4.3.1 PCI Controller Configuration Register Map

The PCI base address for the PCI Controller Configuration Registers is PCI Base Address 0 (PCI Memory Space, Offset 0x10 in the PCI Configuration Space) or PCI Base Address 1 (PCI I/O Space, Offset 0x14 in the PCI Configuration Space).

Do not change hardware dependent bit settings in the PCI Controller Configuration Registers.

Offset from PCI Base Address	Register	Value
0x00	Local Address Space 0 Range	0x0FFF_FFF0
0x04	Local Address Space 1 Range	0x0000_0000
0x08	Local Address Space 2 Range	0x0000_0000
0x0C	Local Address Space 3 Range	0x0000_0000
0x10	Expansion ROM Range	0x0000_0000
0x14	Local Address Space 0 Local Base Address (Remap)	0x0000_0001
0x18	Local Address Space 1 Local Base Address (Remap)	0x0000_0000
0x1C	Local Address Space 2 Local Base Address (Remap)	0x0000_0000
0x20	Local Address Space 3 Local Base Address (Remap)	0x0000_0000
0x24	Expansion ROM Local Base Address (Remap)	0x0000_0000
0x28	Local Address Space 0 Bus Region Descriptor	0x1581_20A0
0x2C	Local Address Space 1 Bus Region Descriptor	0x0000_0000
0x30	Local Address Space 2 Bus Region Descriptor	0x0000_0000
0x34	Local Address Space 3 Bus Region Descriptor	0x0000_0000
0x38	Expansion ROM Bus Region Descriptor	0x0000_0000
0x3C	Chip Select 0 Base Address	0x0000_0009
0x40	Chip Select 1 Base Address	0x0000_0000
0x44	Chip Select 2 Base Address	0x0000_0000
0x48	Chip Select 3 Base Address	0x0000_0000
0x4C	Interrupt Control/Status	0x0041
0x4E	Serial EEPROM Write-Protected Address Boundary	0x0030
0x50	PCI Target Response, Serial EEPROM Control, and Initialization Control	0x1878_4000
0x54	General Purpose I/O Control	0x0020_06D2
0x70	Hidden 1 Register for Power Management Data Select	0x0000_0000
0x74	Hidden 2 Register for Power Management Data Scale	0x0000_0000

Table 4-3 : PCI Controller Configuration Register Map

4.4 Local Register Space

The PCI base address for the Local Registers is PCI Base Address 2 (PCI Memory Space, Offset 0x18 in the PCI Configuration Space).

Offset to BAR2	Register Name	Size (Bit)
0x0000	Data Output Register	32
0x0004	Control Register	32

Table 4-4 : Local Register Space

4.4.1 Data Output Register

The Data Output Register is a long word wide read/write register used to set or clear the outputs lines.

Bit	Symbol	Description	Access	Reset Value
31:0	OUTPUT 32 … OUTPUT 1	Set or clear the corresponding output line 1 = active 0 = inactive Bit 0 represents OUT 1, Bit 31 represents OUT 32 accordingly	R/W	0

Table 4-5 : Data Output Register

After power-on or reset the Data Output Register is cleared to '0', all outputs are inactive.

4.4.2 Control Register

The Control Register is a 32 bit read/write register.

Bit	Symbol	Description	Access	Reset Value
31:4	-	Reserved (0 for reads)	-	0
3	WDOG_STAT	Watchdog Status bit 1 = indicate that the watchdog has recognized a failure and has disabled all output channels. The Data Output Register is locked. Writing '1' to this bit unlocks the Data Output Register. 0 = signals normal operation	R/W	0
2	-	Reserved (0 for reads)	-	0
1	WDOG_EN	Watchdog Enable bit for all 32 outputs 1 = enable watchdog function 0 = disable	R/W	0
0	-	Reserved (0 for reads)	-	0

Table 4-6 : Control Register

The watchdog status is only active if the watchdog is enabled.

4.5 Serial EEPROM Memory

The serial EEPROM memory contains by default the TEWS PCI Interface FPGA configuration data for compatibility reasons. However, the entire configuration data is stored within and loaded from the internal flash of the PCI target chip.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x02BC	0x1498	0x0280	0x0000	0x1180	0x0000	s.b.	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x0001	0x0000	0x0000
0x20	0x0000	0x0006	0x0000	0x0003	0x0FFF	0xFFF0	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x1581	0x20A0	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0009	0x0000	0x0000	0x0000	0x0000
0x70	0x0000	0x0000	0x0030	0x0000	0x0078	0x0000	0x0020	0x06D2
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 4-7 : Configuration EEPROM

Subsystem-ID Value (Offset 0x0C):

TPMC700-10R	0x000A
TPMC700-11R	0x000B
TPMC700-20R	0x0014
TPMC700-21R	0x0015

5 Configuration hints

5.1 Local Software Reset

The Local Reset LRESET# is used to reset the on board local logic.

The Local Reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of ‘1’ resets the local logic. The chip remains in this reset condition until the PCI Host clears this bit. The contents of the PCI and Local Configuration Registers is reset. The PCI Interface is not reset.

6 Functional Description of Digital Outputs

6.1 Optical Isolation

The TPMC700 has 32 (TPMC700-10R/-20R) or 16 (TPMC700-11R/-21R) digital outputs. The standard signal level for these outputs is 24 VDC. All outputs are isolated by optocouplers from the system and in two ground groups (output OUT 1-16 and output OUT 17-32) against each other.

Within these two groups there are four subgroups for the VS power supply which allow different supply voltages in groups of four, but referenced to the same GND.

Group	Supply	Ground	Output
O1	VS_O1	GND_OA	OUT 1 OUT 2 OUT 3 OUT 4
O2	VS_ O2		OUT 5 OUT 6 OUT 7 OUT 8
O3	VS_ O3		OUT 9 OUT 10 OUT 11 OUT 12
O4	VS_ O4		OUT 13 OUT 14 OUT 15 OUT 16
O5	VS_ O5	GND_OB	OUT 17 OUT 18 OUT 19 OUT 20
O6	VS_ O6		OUT 21 OUT 22 OUT 23 OUT 24
O7	VS_ O7		OUT 25 OUT 26 OUT 27 OUT 28
O8	VS_ O8		OUT 29 OUT 30 OUT 31 OUT 32

Table 6-1 : Isolated Digital Outputs summary

6.2 Output Polarity

Each output can be individually switched to the according power supply VS_Ox (high side switch).

6.3 Overload Protection

The output drivers used on the TPMC700 are ‘smart drivers’ TDE1707. The maximum continuous output current is 0.5 A. The output circuits are protected against overload, short circuit and over temperature. In case of such failure the corresponding output is switched off until the error condition is removed. The output returns automatically to normal operation, i.e. the state programmed in the Data Output Register.

6.4 Output Watchdog

Writing ‘1’ into bit 1 of the Control Register the hardware watchdog function is enabled. The status of the watchdog is indicated at bit 3 of the Control Register.

Any software accesses (read or write) to the Data Output Register will retrigger the watchdog. The maximum time between two accesses is set to 120ms. If the time expires without a software access all outputs go into “OFF” state. At the same time the watchdog status will change from ‘0’ to ‘1’ and locks the Data Output Register. This prevents a write access to the Data Output Register. The output register content is not affected by that.

Writing ‘1’ to the watchdog status (bit 3 Control Register) clears this bit and also unlocks the Data Output Register. After unlocking the Data Output Register the output stays in the “OFF” state till the next write access to this register.

The watchdog is disabled after power-on or reset.

7 Programming Hints

7.1 Local Read/Write

The local register set supports long word (32 bit) read/write access only. A byte or word access will fail.

Use only long word read/write accesses to the TPMC700.

8 Installation

8.1 Output Wiring

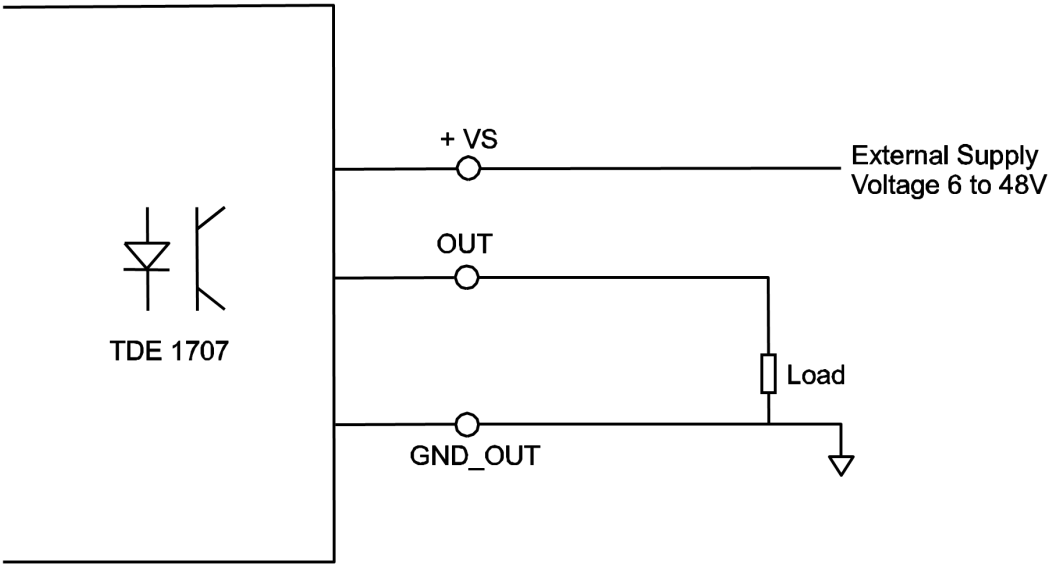

Figure 8-1 : Output Wiring

9 Pin Assignment – I/O Connector

9.1 Front Panel I/O

9.1.1 HD50 Connector

AMP 787395-5 or compatible.

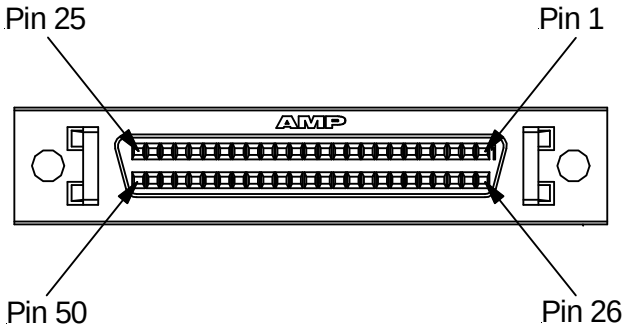

Figure 9-1 : Front Panel I/O Connector Numbering

9.1.2 Front Panel I/O Assignment TPMC700-1xR

The subsequent figure shows the complete assembled pin front panel I/O connector. Bear in mind that variant -11R does not provide the channels 16 up to 32. Consequently, these are unconnected.

Pin	Signal
1	VS_O1
2	VS_O1
3	VS_O2
4	VS_O2
5	VS_O3
6	VS_O3
7	VS_O4
8	VS_O4
9	VS_O5
10	VS_O5
11	VS_O6
12	VS_O6
13	VS_O7
14	VS_O7
15	VS_O8
16	VS_O8
17	OUT 1
18	OUT 2
19	OUT 3
20	OUT 4
21	OUT 5
22	OUT 6
23	OUT 7
24	OUT 8
25	OUT 9

Pin	Signal
26	OUT 10
27	OUT 11
28	OUT 12
29	OUT 13
30	OUT 14
31	OUT 15
32	OUT 16
33	OUT 17
34	OUT 18
35	OUT 19
36	OUT 20
37	OUT 21
38	OUT 22
39	OUT 23
40	OUT 24
41	OUT 25
42	OUT 26
43	OUT 27
44	OUT 28
45	OUT 29
46	OUT 30
47	OUT 31
48	OUT 32
49	GND_OA
50	GND_OB

Table 9-1 : Pin Assignment Front I/O Connector TPMC700-1xR

Please check the maximum current of the used connection cable. Some standard cables (AWG28 50 pol.) are limited to 0.75 A per lead.

9.2 Back panel I/O

9.2.1 Mezzanine Card Connector P14

MOLEX 71436-216 or compatible.

9.2.2 Rear I/O Assignment TPMC700-2xR

The subsequent figure shows the complete Rear I/O connector. Bear in mind that variant -21R does not provide the channels 16 up to 32. Consequently, these are unconnected.

Pin	Signal
1	VS_O1
2	VS_O1
3	VS_O2
4	VS_O2
5	VS_O3
6	VS_O3
7	VS_O4
8	VS_O4
9	VS_O5
10	VS_O5
11	VS_O6
12	VS_O6
13	VS_O7
14	VS_O7
15	VS_O8
16	VS_O8
17	OUT 1
18	OUT 2
19	OUT 3
20	OUT 4
21	OUT 5
22	OUT 6
23	OUT 7
24	OUT 8
25	OUT 9
26	OUT 10

Pin	Signal
27	OUT 11
28	OUT 12
29	OUT 13
30	OUT 14
31	OUT 15
32	OUT 16
33	OUT 17
34	OUT 18
35	OUT 19
36	OUT 20
37	OUT 21
38	OUT 22
39	OUT 23
40	OUT 24
41	OUT 25
42	OUT 26
43	OUT 27
44	OUT 28
45	OUT 29
46	OUT 30
47	OUT 31
48	OUT 32
49	GND_OA
50	GND_OB
51	NC
52 … 64	NC

Table 9-2 : Pin Assignment Rear I/O Connector TPMC700-2xR