The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC682

3 x 16 bit I/O Ports with
512 Word FIFO and Handshake

Version 1.0

User Manual

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TPMC682-10R

3 x 16 bit I/O Ports with
512 Word FIFO and Handshake

HD68 front panel connector

P14 Back I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	April 2005
1.1	New address TEWS LLC	September 2006
1.0.2	New Notation for User Manual and Engineering Documentation	August 2011
1.0.3	General Revision	August 2014

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1 Product Description

The TPMC682 is a standard single-width 32 bit PMC with three 16 bit TTL digital input/output lines controlled by handshake signals. These handshake signals run over an additional 8 bit input and an 8 bit output port. Interlocked or pulsed handshake protocol is provided. Each I/O port has a 512 words deep FIFO. All I/O lines are protected by bus transceivers and ESD protection devices.

The PLX PCI9030 PCI target chip is used for the PCI interface.

An interrupt can be generated on INTA, when the filling level of a FIFO exceeds the value of the individually programmable threshold. Each port has a programmable timeout counter for input direction of data.

The TPMC682 provides front panel I/O via a HD68 SCSI-3 type connector and rear panel I/O via P14 (Port 2 not fully supported over back I/O).

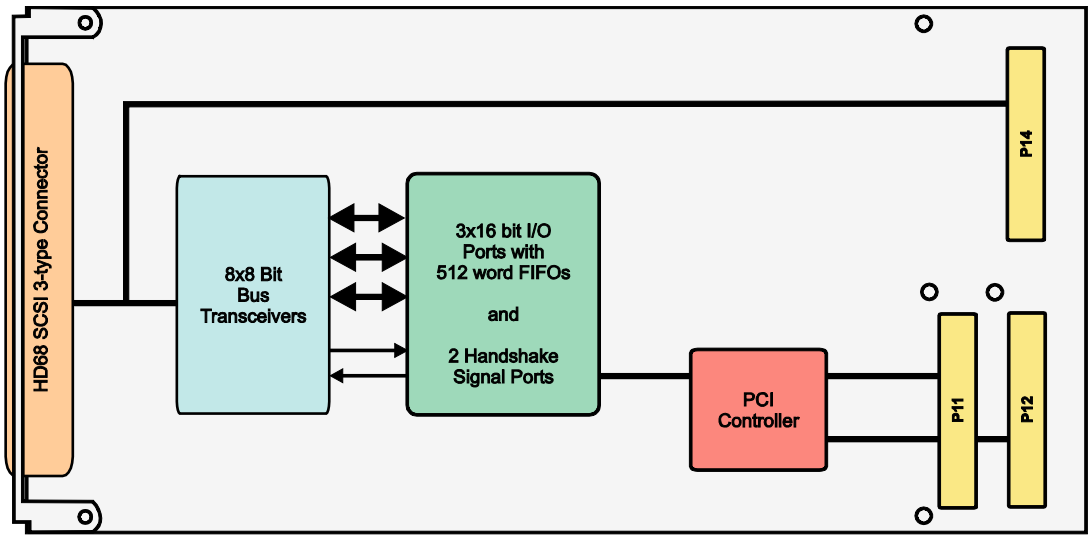

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface	
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size
Electrical Interface	PCI Rev. 2.1 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage
On Board Devices	
PCI Target Chip	PCI9030 (PLX Technology)
Local Control Logic	FPGA Spartan2 XC2S100-5 FG256 I (Xilinx)
I/O Interface	
Number of I/O Lines	64 lines arranged in 3 x 16 bit handshake ports (Port 0-2) and 2 x 8 bit ports (Port 4/5) for handshake signals, Max. output current per line: -8mA (High level) 8mA (Low level)
I/O Connector	PMC P14 I/O (64pin Mezzanine Connector): all ports, except for upper byte of port 2 (can be changed to all signals of Port 2, without ground lines) Front panel HD68 SCSI-3 type Connector: all ports
Physical Data	
Power Requirements	100mA typical @ +3.3V DC 70mA typical (no load) @ +5V DC
Temperature Range	Operating -40 °C to +85 °C Storage -40°C to +125°C
MTBF	373000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	74 g

Table 2-1 : Technical Specification

3 Handshake Mode

There are three 16 bit ports available (Port 0 - 2), input and output transfers are buffered by FIFOs, each 512 words deep. Buffering allows orderly transfers by using the handshake pins in one of two programmable protocols.

Use of buffering is most beneficial in situations where a peripheral device and the computer system are capable of transferring data at roughly the same speed. Buffering allows the write operation of the data transmitter to be overlapped with the fetch operation of the data receiving device. Thus, throughput may be greatly enhanced. If there is a large mismatch in transfer capability between the computer and the peripheral, little or no benefit is obtained. In these cases there is no penalty in using buffering.

Port 4 is an input port, bit 0, 1 and 2 of port 4 are used as handshake input signals H1/H3/H5.

Port 5 is an output port, bit 0, 1 and 2 are the handshake output signals H2/H4/H6. The action is programmable.

The FIFO_STATUS0/1/2 flag, which is bit 7 of the Handshake Status and Control Registers HSCR0/1/2, gives information about the fill status of the FIFO. An interrupt is triggered if FIFO_STATUS0/1/2 flag is set and it is enabled by bit 1 of Handshake Status and Control Register HSCR0/1/2 as well as the global interrupt is enabled: bit 0 of IFCR.

H1 and H2 belong to the 16 bit port on port 0, H3/H4 belong to port 1 and H5/H6 belong to port 2.

Handshake Input Signals	H1: Port 4 Line 0 H3: Port 4 Line 1 H5: Port 4 Line 2
Handshake Output Signals	H2: Port 5 Line 0 H4: Port 5 Line 1 H6: Port 5 Line 2

Input Transfers:

If input direction is set for a handshake port, H1 (H3/H5) input signal is used for acquisition of data. Data is buffered on a falling edge of H1 (H3/H5). FIFO_STATUS0/1/2 is set when the number of stored data words in the FIFO exceeds the value specified by the corresponding FIFO threshold register FTHR0/1/2. If the handshake output signals H2 (H4/H6) are used, they indicate whether there is room for more data in the FIFO or not.

If H2 (H4/H6) output is used, it may be in the interlocked or pulsed input handshake protocol. The protocol is set by bit 5 and 6 of the Handshake Status and Control Registers HSCR0/1/2.

In the interlocked input handshake protocol signal H2 (H4/H6) is cleared when the port input buffers are ready to accept new data. It is set following the falling edge of the H1 (H3/H5) input. When ready for new data, H2 (H4/H6) is cleared again. When FIFO is full H2 (H4/H6) remains high until data is removed by a read of port data register. Thus, anytime H2 (H4/H6) output is low, new input data may be entered by a falling edge on H1 (H3/H5). At other times transitions of H1 (H3/H5) are ignored.

In the pulsed input handshake protocol signal H2 (H4/H6) is cleared in the same way as in the interlocked input protocol, but never remains low longer than four clock cycles. Typically a four-clock cycle pulse is generated. But in the case that a subsequent H1 (H3/H5) falling edge occurs before termination of the pulse, H2 (H4/H6) is set immediately high. Thus, anytime after a falling edge of the H2 (H4/H6) pulse, new data may be entered in the buffers.

A timeout function can signal when no data was received for a specified timeout period. It is realized by a counter which is clocked with 1/33 of the PCI clock frequency, normally about 1 MHz (or 1µs period time). The timeout period is specified by the 16 bit preload value of the timeout (downward-) counter in the Timeout Counter Preload Registers TCPR0/1/2, i.e.: the maximum timeout period is about 65ms. The timeout function is started after the first asserted edge on the corresponding handshake input line after enabling by setting bit TOUT_EN0/1/2 and is retriggered with every following edge. When data receiving is stopped because of a filled FIFO, no timeout event is generated. An interrupt is triggered if TOUT_STATUS0/1/2 flag is set and it is enabled by bit 1 of Handshake Status and Control Register HSCR0/1/2 as well as the global interrupt is enabled: bit 0 of IFCR.

In the figure below “Input Transfer Timing Diagram” a sample timing diagram is given. The H2 (H4/H6) interlocked and pulse input handshake protocols are shown.

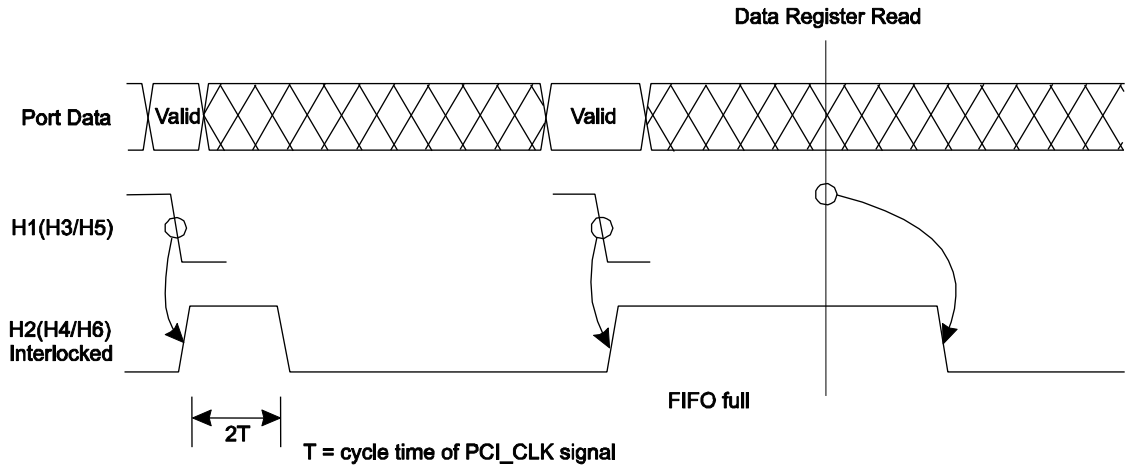

Figure 3-1 : Input Transfer Timing Diagram

Output Transfers:

The peripheral accepts the data by a falling edge on H1 (H3/H5), which causes the next word to be moved to the corresponding output. H2 (H4/H6) indicates that new data has been moved to the output.

If H2 (H4/H6) output is used, it may be in the interlocked or pulsed output handshake protocol. The protocol is set by bit 5 and 6 of the Handshake Status and Control Registers HSCR0/1/2.

In the interlocked output handshake protocol signal H2 (H4/H6) is cleared two clock cycles after data is transferred to the output. The data remains stable and H2 (H4/H6) remains low until the next falling edge of the H1 (H3/H5) input. At that time H2 (H4/H6) goes high. As soon as the next data is available, it is transferred to the output and H2 (H4/H6) is cleared again. When H2 (H4/H6) is high, transitions on H1 (H3/H5) have no effect.

When H2 (H4/H6) is an output pin in the pulsed output handshake protocol, it is cleared exactly as in the interlocked output protocol, but never remains low longer than four clock cycles. Typically a four-clock cycle pulse is generated. But in case that a subsequent H1 (H3/H5) falling edge occurs before termination of the pulse, H2 (H4/H6) is set immediately high, thus shortening the pulse.

The FIFO_STATUS0/1/2 status bit is high when the fill level of the FIFO falls below the value specified in the corresponding threshold register.

The typical delay time between a falling edge on H1 (H3/H5) and the next falling edge on H2 (H4/H6) signaling new valid output data, is about 180ns.

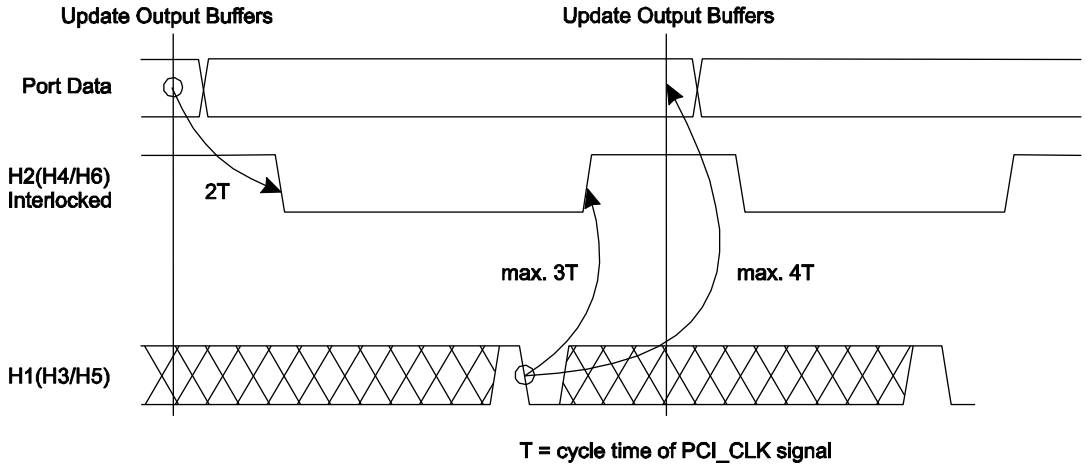

Figure 3-2 : Output Transfer Timing Diagram

4 Local Space Addressing

4.1 PCI9030 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9030 local spaces.

PCI9030 Local Space	PCI9030 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	2 (0x18)	MEM	64	32	BIG	FPGA Control Register Address Space
1	3 (0x1C)	MEM	16	16	BIG	FPGA Port Register Address Space
2	4 (0x20)	-	-	-	-	Not Used
3	5 (0x24)	-	-	-	-	Not Used

Table 4-1 : PCI9030 Local Space Configuration

4.2 FPGA Control Register Space

PCI Base Address: **PCI9030 PCI Base Address 2 (Offset 0x18 in PCI Configuration Space).**

Offset to PCI Base Address 2	Register Name	Size (Bit)
0x00	INTERRUPT AND FIFO CONTROL REGISTER (IFCR)	32
0x04	PORT DATA DIRECTION REGISTER (PDDR)	32
0x08 ... 0x10	Reserved	-
0x11	HANDSHAKE STATUS AND CONTROL REGISTER 2 (HSCR2)	8
0x12	HANDSHAKE STATUS AND CONTROL REGISTER 1 (HSCR1)	8
0x13	HANDSHAKE STATUS AND CONTROL REGISTER 0 (HSCR0)	8
0x14	TIMEOUT COUNTER PRELOAD REGISTER 2 (TCPR2)	32
0x18	TIMEOUT COUNTER PRELOAD REGISTER 1 (TCPR1)	32
0x1C	TIMEOUT COUNTER PRELOAD REGISTER 0 (TCPR0)	32
0x20	FIFO DATA COUNTER REGISTER 2 (FDCR2)	32
0x24	FIFO DATA COUNTER REGISTER 1 (FDCR1)	32
0x28	FIFO DATA COUNTER REGISTER 0 (FDCR0)	32
0x2C…0x2F	Reserved	-
0x30	FIFO THRESHOLD REGISTER 2 (FTHR2)	32
0x34	FIFO THRESHOLD REGISTER 1 (FTHR1)	32
0x38	FIFO THRESHOLD REGISTER 0 (FTHR0)	32
0x3C…0x3F	Reserved	-

Table 4-2 : Control Register Space

4.2.1 Interrupt and FIFO Control Register (IFCR; 0x00)

Bit	Symbol	Description	Access	Reset Value
31..8	-	Reserved (0 for reads)	-	0
7	FIFO_FLUSH	FIFO Flush Request 0 : no FIFO Flush Request 1 : Flush all FIFOs (bit is automatically reset)	R/W	0
6..1	-	Reserved (0 for reads)	-	0
0	GLOB_INT_EN	Global Interrupt Enable 0 : Interrupts disabled 1 : Interrupts enabled	R/W	0

Table 4-3 : Interrupt and FIFO Control Register (IFCR)

4.2.2 Port Data Direction Register (PDDR; 0x04)

All 8/16 lines of one port have the same direction.

Bit	Symbol	Description	Access	Reset Value
31: 8	-	Reserved (0 for reads)	-	0
7	HS-PORT2_DIR	Port 2 Data Direction 0 : Port is Input 1 : Port is Output	R	00
6			R/W	
5	PORT5_DIR	Port 5 Data Direction, always output	R	1
4	PORT4_DIR	Port 4 Data Direction, always input	R	0
3	HS-PORT1_DIR	Port 0 / 1 Data Direction 0 : Port is Input 1 : Port is Output	R	00
2			R/W	
1	HS-PORT0_DIR		R	00
0			R/W	

Table 4-4 : Port Data Direction Register (PDDR)

The direction of port 4 is always input because of H1/H3/H5. The direction of port 5 is output because of H2/H4/H6.

Bit 1 has always the same value as bit 0, this also applies to bits 2/3 and 6/7 (use bits 0, 2, 6 to specify the direction of a 16 bit port).

4.2.3 Handshake Status and Control Register 2 (HSCR2; 0x11)

See chapter “Handshake Mode” for a description of the mode and the configuration bits in the Handshake Status and Control Registers.

Bit	Symbol	Description	Access	Reset Value
7	FIFO_STATUS2	FIFO Status Flag 0 : FIFO level within threshold of FTHR2 1 : FIFO level exceeds threshold of FTHR2	R	0
6..5	PORT2_HS	H6 Handshake Output Protocol 00 : none 10 : Interlocked Handshake Protocol 11 : Pulsed Handshake Protocol	R/W	00
4	TOUT_STATUS2	Read Timeout Status Flag 0 : no Timeout Event 1 : active Timeout Event	R/W	0
3	TOUT_EN2	Read Timeout Enable 0 : Read Timeout Counter halted 1 : Read Timeout Counter enabled	R/W	0
2	-	Reserved (‘0’ for reads)	-	0
1	INT_EN2	Port 2 Interrupt Enable 0 : Interrupts disabled 1 : Interrupts enabled	R/W	0
0	-	Reserved (‘1’ for reads)	-	1

Table 4-5 : Handshake Status and Control Register 2 (HSCR2)

The Handshake Status and Control Register 2 controls 16 bit Handshake Port 2.

After the Timeout Counter is enabled, it is started with the first falling edge on H5.

When interrupts are enabled globally (bit 0 of IFCR is ‘1’) and for Port 2 (bit 1 is ‘1’), an interrupt is generated when Timeout Status Flag is ‘1’ or FIFO Status Flag is ‘1’.

The Timeout Status Flag is acknowledged by writing ‘1’ to bit 4.

4.2.4 Handshake Status and Control Register 1 (HSCR1; 0x12)

Bit	Symbol	Description	Access	Reset Value
7	FIFO_STATUS1	FIFO Status Flag 0 : FIFO level within threshold of FTHR1 1 : FIFO level exceeds threshold of FTHR1	R	0
6..5	PORT1_HS	H4 Handshake Output Protocol 00 : none 10 : Interlocked Handshake Protocol 11 : Pulsed Handshake Protocol	R/W	00
4	TOUT_STATUS1	Read Timeout Status Flag 0 : no Timeout Event 1 : active Timeout Event	R/W	0
3	TOUT_EN1	Read Timeout Enable 0 : Read Timeout Counter halted 1 : Read Timeout Counter enabled	R/W	0
2	-	Reserved (‘0’ for reads)	-	0
1	INT_EN1	Port 1 Interrupt Enable 0 : Interrupts disabled 1 : Interrupts enabled	R/W	0
0	-	Reserved (‘1’ for reads)	-	1

Table 4-6 : Handshake Status and Control Register 1 (HSCR1)

The Handshake Status and Control Register 1 controls 16 bit Handshake Port 1.

After the Timeout Counter is enabled, it is started with the first falling edge on H3.

When interrupts are enabled globally (bit 0 of IFCR is ‘1’) and for Port 1 (bit 1 is ‘1’), an interrupt is generated when Timeout Status Flag is ‘1’ or FIFO Status Flag is ‘1’.

The Timeout Status Flag is acknowledged by writing ‘1’ to bit 4.

4.2.5 Handshake Status and Control Register 0 (HSCR0; 0x13)

Bit	Symbol	Description	Access	Reset Value
7	FIFO_STATUS0	FIFO Status Flag 0 : FIFO level within threshold of FTHR0 1 : FIFO level exceeds threshold of FTHR0	R	0
6..5	PORT0_HS	H2 Handshake Output Protocol 00 : None 10 : Interlocked Handshake Protocol 11 : Pulsed Handshake Protocol	R/W	00
4	TOUT_STATUS0	Read Timeout Status Flag 0 : no Timeout Event 1 : active Timeout Event	R/W	0
3	TOUT_EN0	Read Timeout Enable 0 : Read Timeout Counter halted 1 : Read Timeout Counter enabled	R/W	0
2	-	Reserved (‘0’ for reads)	-	0
1	INT_EN0	Port 0 Interrupt Enable 0 : Interrupts disabled 1 : Interrupts enabled	R/W	0
0	-	Reserved (‘1’ for reads)	-	1

Table 4-7 : Handshake Status and Control Register 0 (HSCR0)

The Handshake Status and Control Register 0 controls 16 bit Handshake Port 0.

After the Timeout Counter is enabled, it is started with the first falling edge on H1.

When interrupts are enabled globally (bit 0 of IFCR is ‘1’) and for Port 0 (bit 1 is ‘1’), an interrupt is generated when Timeout Status Flag is ‘1’ or FIFO Status Flag is ‘1’.

The Timeout Status Flag is acknowledged by writing ‘1’ to bit 4.

4.2.6 Timeout Counter Preload Register 2 (TCPR2; 0x14)

Bit	Symbol	Description	Access	Reset Value
31..16	-	Reserved (0 for reads)	-	0
15..0	TOUT_CNTRPREL2	Timeout Value for Read Access (multiply value with 33 times the PCI cycle time for resulting timeout delay time)	R/W	0x00FF

Table 4-8 : FIFO Threshold Register 2 (FTHR2)

4.2.7 Timeout Counter Preload Register 1 (TCPR1; 0x18)

Bit	Symbol	Description	Access	Reset Value
31..16	-	Reserved (0 for reads)	-	0
15..0	TOUT_CNTRPREL1	Timeout Value for Read Access (multiply value with 33 times the PCI cycle time for resulting timeout delay time)	R/W	0x00FF

Table 4-9 : FIFO Threshold Register 1 (FTHR1)

4.2.8 Timeout Counter Preload Register 0 (TCPR0; 0x1C)

Bit	Symbol	Description	Access	Reset Value
31..16	-	Reserved (0 for reads)	-	0
15..0	TOUT_CNTRPREL0	Timeout Value for Read Access (multiply value with 33 times the PCI cycle time for resulting timeout delay time)	R/W	0x00FF

Table 4-10: FIFO Threshold Register 0 (FTHR0)

4.2.9 FIFO Data Counter Register 2 (FDCR2; 0x20)

Bit	Symbol	Description	Access	Reset Value
31..10	-	Reserved (0 for reads)	-	0
9..0	FIFO_CNTR2	Amount of data words in FIFO 2	R	0x000

Table 4-11: FIFO Data Counter Register 2 (FDCR2)

4.2.10 FIFO Data Counter Register 1 (FDCR1; 0x24)

Bit	Symbol	Description	Access	Reset Value
31..10	-	Reserved (0 for reads)	-	0
9..0	FIFO_CNTR1	Amount of data words in FIFO 1	R	0x000

Table 4-12: FIFO Data Counter Register 1 (FDCR1)

4.2.11 FIFO Data Counter Register 0 (FDCR0; 0x28)

Bit	Symbol	Description	Access	Reset Value
31..10	-	Reserved (0 for reads)	-	0
9..0	FIFO_CNTR0	Amount of data words in FIFO 0	R	0x000

Table 4-13: FIFO Data Counter Register 0 (FDCR0)

4.2.12 FIFO Threshold Register 2 (FTHR2; 0x30)

Bit	Symbol	Description	Access	Reset Value
31..10	-	Reserved (0 for reads)	-	0
9..0	FIFO_FTR2	Threshold of FIFO 2 for setting of FIFO_STATUS2	R/W	0x040

Table 4-14: FIFO Threshold Register 2 (FTHR2)

4.2.13 FIFO Threshold Register 1 (FTHR1; 0x34)

Bit	Symbol	Description	Access	Reset Value
31..10	-	Reserved (0 for reads)	-	0
9..0	FIFO_FTR1	Threshold of FIFO 1 for setting of FIFO_STATUS1	R/W	0x040

Table 4-15: FIFO Threshold Register 1 (FTHR1)

4.2.14 FIFO Threshold Register 0 (FTHR0; 0x38)

Bit	Symbol	Description	Access	Reset Value
31..10	-	Reserved (0 for reads)	-	0
9..0	FIFO_FTR0	Threshold of FIFO 0 for setting of FIFO_STATUS0	R/W	0x040

Table 4-16: FIFO Threshold Register 0 (FTHR0)

The threshold values should be greater than '0', for proper function.

4.3 FPGA Port Register Space

PCI Base Address:	PCI9030 PCI Base Address 3 (Offset 0x1C in PCI Configuration Space).

Offset to PCI Base Address 3	Register Name	Size (Bit)	Access Width (Bit)
0x0 (or 0x2)	HS-PORT 2 DATA REGISTER (PDR2)	16	16/32
0x4 (or 0x6)	HS-PORT 1 DATA REGISTER (PDR1)	16	16/32
0x8 (or 0xA)	HS-PORT 0 DATA REGISTER (PDR0)	16	16/32
0xC	PORT DATA REGISTER 5 (PDR5), output	8	8/16/32
0xD	PORT DATA REGISTER 4 (PDR4), input	8	8/16/32
0xE ... 0xF	Reserved	-	

Table 4-17: Port Register Space

4.3.1 HS-Port Data Register 2 (PDR2; 0x0 or 0x2)

Bit	Symbol	Description	Access	Reset Value
15	PORT2_BIT_15	Port 2 bit 0-15	R/W	0
14	PORT2_BIT_14			
13	PORT2_BIT_13			
12	PORT2_BIT_12			
11	PORT2_BIT_11			
10	PORT2_BIT_10			
9	PORT2_BIT_9			
8	PORT2_BIT_8			
7	PORT2_BIT_7			
6	PORT2_BIT_6			
5	PORT2_BIT_5			
4	PORT2_BIT_4			
3	PORT2_BIT_3			
2	PORT2_BIT_2			
1	PORT2_BIT_1			
0	PORT2_BIT_0			

Table 4-18: HS-Port Data Register 2

For performance reasons it might be useful to read/write 32 bit lwords at once over the PCI bus to the FIFOs. They will be split into two 16 bit word accesses after another; the word with the lower address will be read/written at first to/from the FIFO (see example in next figure).

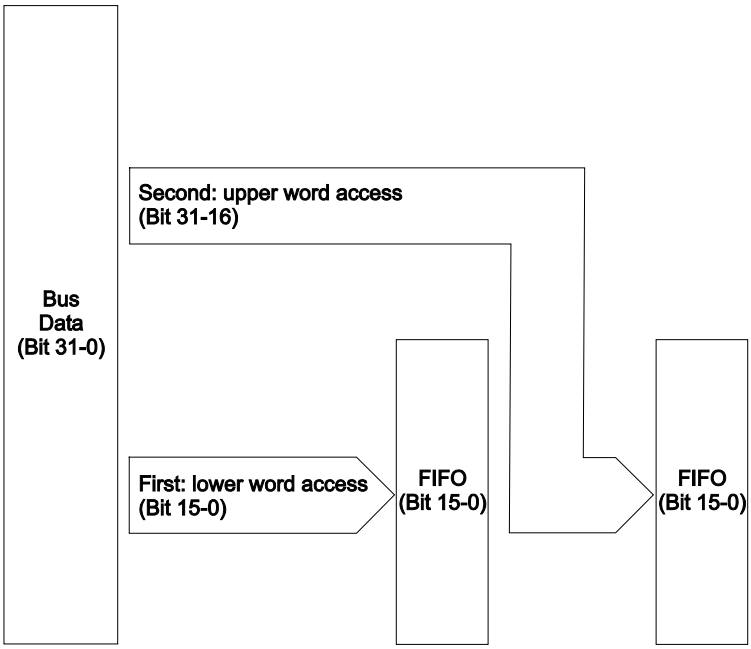

Figure 4-1 : Example of a 32 Bit Port Data Register Write Access

4.3.2 HS-Port Data Register 1 (PDR1; 0x4 or 0x6)

Bit	Symbol	Description	Access	Reset Value
15	PORT1_BIT_15	Port 1 bit 0-15	R/W	0
14	PORT1_BIT_14			
13	PORT1_BIT_13			
12	PORT1_BIT_12			
11	PORT1_BIT_11			
10	PORT1_BIT_10			
9	PORT1_BIT_9			
8	PORT1_BIT_8			
7	PORT1_BIT_7			
6	PORT1_BIT_6			
5	PORT1_BIT_5			
4	PORT1_BIT_4			
3	PORT1_BIT_3			
2	PORT1_BIT_2			
1	PORT1_BIT_1			
0	PORT1_BIT_0			

Table 4-19: HS-Port Data Register 1

4.3.3 HS-Port Data Register 0 (PDR0; 0x8 or 0xA)

Bit	Symbol	Description	Access	Reset Value
15	PORT0_BIT_15	Port 0 bit 0-15	R/W	0
14	PORT0_BIT_14			
13	PORT0_BIT_13			
12	PORT0_BIT_12			
11	PORT0_BIT_11			
10	PORT0_BIT_10			
9	PORT0_BIT_9			
8	PORT0_BIT_8			
7	PORT0_BIT_7			
6	PORT0_BIT_6			
5	PORT0_BIT_5			
4	PORT0_BIT_4			
3	PORT0_BIT_3			
2	PORT0_BIT_2			
1	PORT0_BIT_1			
0	PORT0_BIT_0			

Table 4-20: HS-Port Data Register 0

4.3.4 Port Data Register 5 (PDR5; 0xC)

Bit	Symbol	Description	Access	Reset Value
7	PORT5_BIT_7	Port 5 bit 3-7 Data	R/W	0
6	PORT5_BIT_6			
5	PORT5_BIT_5			
4	PORT5_BIT_4			
3	PORT5_BIT_3			
2	PORT5_BIT_2	Handshake output signal H6	R/W	0
1	PORT5_BIT_1	Handshake output signal H4	R/W	0
0	PORT5_BIT_0	Handshake output signal H2	R/W	0

Table 4-21: Port Data Register 5 (PDR5)

4.3.5 Port Data Register 4 (PDR4; 0xD)

Bit	Symbol	Description	Access	Reset Value
7	PORT4_BIT_7	Port 4 bit 3-7 input data	R	-
6	PORT4_BIT_6			
5	PORT4_BIT_5			
4	PORT4_BIT_4			
3	PORT4_BIT_3			
2	PORT4_BIT_2	Handshake input signal H5	R	-
1	PORT4_BIT_1	Handshake input signal H3	R	-
0	PORT4_BIT_0	Handshake input signal H1	R	-

Table 4-22: Port Data Register 4 (PDR4)

5 PCI9030 Target Chip

5.1 PCI Configuration Registers (PCR)

5.1.1 PCI9030 Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits								PCI writeable	Initial Values (Hex Values)
	31	24	23	16	15	8	7	0		
0x00	Device ID				Vendor ID				N	02AA 1498
0x04	Status				Command				Y	0280 0000
0x08	Class Code						Revision ID		N	118000 00
0x0C	BIST		Header Type		PCI Latency Timer		Cache Line Size		Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers								Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers								Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0								Y	FFFFFFC0
0x1C	PCI Base Address 3 for Local Address Space 1								Y	FFFFFFF0
0x20	PCI Base Address 4 for Local Address Space 2								Y	00000000
0x24	PCI Base Address 5 for Local Address Space 3								Y	00000000
0x28	PCI CardBus Information Structure Pointer								N	00000000
0x2C	Subsystem ID				Subsystem Vendor ID				N	000A 1498
0x30	PCI Base Address for Local Expansion ROM								Y	00000000
0x34	Reserved						New Cap. Ptr.		N	000000 40
0x38	Reserved								N	00000000
0x3C	Max_Lat		Min_Gnt		Interrupt Pin		Interrupt Line		Y[7:0]	00 00 01 00
0x40	PM Cap.				PM Nxt Cap.		PM Cap. ID		N	4801 00 01
0x44	PM Data		PM CSR EXT		PM CSR				Y	00 00 0000
0x48	Reserved		HS CSR		HS Nxt Cap.		HS Cap. ID		Y[23:16]	00 00 00 06
0x4C	VPD Address				VPD Nxt Cap.		VPD Cap. ID		Y[31:16]	0000 00 03
0x50	VPD Data								Y	00000000

Table 5-1 : PCI9030 Header

5.1.2 PCI Base Address Initialization

PCI Base Address Initialization is scope of the PCI host software.

PCI9030 PCI Base Address Initialization:

1. Write 0xFFFF_FFFF to the PCI9030 PCI Base Address Register.
2. Read back the PCI9030 PCI Base Address Register.
3. For PCI Base Address Registers 0:5, check bit 0 for PCI Address Space:

   Bit 0 = '0' requires PCI Memory Space mapping

   Bit 0 = '1' requires PCI I/O Space mapping

   For the PCI Expansion ROM Base Address Register, check bit 0 for usage:

   Bit 0 = '0': Expansion ROM not used

   Bit 0 = '1': Expansion ROM used
4. For PCI I/O Space mapping, starting at bit location 2, the first bit set determines the size of the required PCI I/O Space size.

   For PCI Memory Space mapping, starting at bit location 4, the first bit set to '1' determines the size of the required PCI Memory Space size.

   For PCI Expansion ROM mapping, starting at bit location 11, the first bit set to '1' determines the required PCI Expansion ROM size.

   For example, if bit 5 of a PCI Base Address Register is detected as the first bit set to '1', the PCI9030 is requesting a 32 byte space (address bits 4:0 are not part of base address decoding).
5. Determine the base address and write the base address to the PCI9030 PCI Base Address Register. For PCI Memory Space mapping the mapped address region must comply with the definition of bits 3:1 of the PCI9030 PCI Base Address Register.

After programming the PCI9030 PCI Base Address Registers, the software must enable the PCI9030 for PCI I/O and/or PCI Memory Space access in the PCI9030 PCI Command Register (Offset 0x04). To enable PCI I/O Space access to the PCI9030, set bit 0 to '1'. To enable PCI Memory Space access to the PCI9030, set bit 1 to '1'.

Offset in Config.	Description	Usage
0x10	PCI9030 LCR's MEM	Used
0x14	PCI9030 LCR's I/O	Used
0x18	PCI9030 Local Space 0	Used
0x1C	PCI9030 Local Space 1	Used
0x30	Expansion ROM	Not used

Table 5-2 : PCI9030 PCI Base Address Usage

5.2 Local Configuration Register (LCR)

After reset, the PCI9030 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

The PCI base address for the PCI9030 Local Configuration Registers is PCI9030 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9030 PCI Configuration Register Space) or PCI9030 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9030 PCI Configuration Register Space).

Do not change hardware dependent bit settings in the PCI9030 Local Configuration Registers.

Offset from PCI Base Address	Register	Value	Description
0x00	Local Address Space 0 Range	0x0FFF_FFC0	FPGA Control Address Space
0x04	Local Address Space 1 Range	0x0FFF_FFF0	FPGA Port Address Space
0x08	Local Address Space 2 Range	0x0000_0000	
0x0C	Local Address Space 3 Range	0x0000_0000	
0x10	Local Exp. ROM Range	0x0000_0000	
0x14	Local Re-map Register Space 0	0x0000_0001	
0x18	Local Re-map Register Space 1	0x0000_0041	
0x1C	Local Re-map Register Space 2	0x0000_0000	
0x20	Local Re-map Register Space 3	0x0000_0000	
0x24	Local Re-map Register ROM	0x0000_0000	
0x28	Local Address Space 0 Descriptor	0x1581_20A0	
0x2C	Local Address Space 1 Descriptor	0x0540_20A0	
0x30	Local Address Space 2 Descriptor	0x0000_0000	
0x34	Local Address Space 3 Descriptor	0x0000_0000	
0x38	Local Exp. ROM Descriptor	0x0000_0000	
0x3C	Chip Select 0 Base Address	0x0000_0081	
0x40	Chip Select 1 Base Address	0x0000_0000	
0x44	Chip Select 2 Base Address	0x0000_0000	
0x48	Chip Select 3 Base Address	0x0000_0000	
0x4C	Interrupt Control/Status	0x0041	
0x4E	EEPROM Write Protect Boundary	0x0030	
0x50	Miscellaneous Control Register	0x0078_0000	
0x54	General Purpose I/O Control	0x0024_96C0	
0x70	Hidden1 Power Management data select	0x0000_0000	
0x74	Hidden 2 Power Management data scale	0x0000_0000	

Table 5-3 : PCI9030 Local Configuration Register

5.3 Configuration EEPROM

After power-on or PCI reset the PCI9030 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x27 : PCI9030 PCI Configuration Register Values
- Address 0x28 to 0x87 : PCI9030 Local Configuration Register Values
- Address 0x88 to 0xFF : Reserved

See the PCI9030 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x02AA	0x1498	0x0280	0x0000	0x1180	0x0000	0x000A	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x0001	0x0000	0x0000
0x20	0x0000	0x0006	0x0000	0x0003	0x0FFF	0xFFC0	0x0FFF	0xFFF0
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x0041	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x1581	0x20A0	0x0540	0x20A0	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0081	0x0000	0x0000	0x0000	0x0000
0x70	0x0000	0x0000	0x0030	0x0041	0x0078	0x0000	0x0024	0x96C0
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 5-4 : Configuration EEPROM

5.4 Local Software Reset

The PCI9030 Local Reset Output LRESETo# is used to reset the on board local logic.

The PCI9030 local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the PCI9030 local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of 1 resets the PCI9030 and issues a reset to the Local Bus (LRESETo# asserted). The PCI9030 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI9030 PCI and Local Configuration Registers are not reset. The PCI9030 PCI Interface is not reset.

6 Configuration Hints

6.1 Big / Little Endian

PCI – Bus (Little Endian)

Byte 0	AD[7..0]
Byte 1	AD[15..8]
Byte 2	AD[23..16]
Byte 3	AD[31..24]

Every Local Address Space (0...3) and the Expansion ROM Space can be programmed to operate in Big or Little Endian Mode.

Big Endian		**Little Endian**	
32 Bit		**32 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
Byte 2	D[15..8]	Byte 2	D[23..16]
Byte 3	D[7..0]	Byte 3	D[31..24]
16 Bit upper lane		**16 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
16 Bit lower lane			
Byte 0	D[15..8]		
Byte 1	D[7..0]		
8 Bit upper lane		**8 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
8 Bit lower lane			
Byte 0	D[7..0]		

Table 6-1 : Local Bus Little/Big Endian

Standard use of the TPMC682 design:

Local Address Space 0	32 bit bus in Big Endian Mode
Local Address Space 1	16 bit bus in Big Endian Mode
Local Address Space 2	not used
Local Address Space 3	not used
Expansion ROM Space	not used

To change the Endian Mode use the Local Configuration Registers for the corresponding Space. Bit 24 of the according register sets the mode. A value of 1 indicates Big Endian and a value of 0 indicates Little Endian.

Use the PCI Base Address 0 + Offset or PCI Base Address 1 + Offset:

Short cut	Offset	Name
LAS0BRD	0x28	Local Address Space 0 Bus Region Description Register
LAS1BRD	0x2C	Local Address Space 0 Bus Region Description Register
LAS2BRD	0x30	Local Address Space 0 Bus Region Description Register
LAS3BRD	0x34	Local Address Space 0 Bus Region Description Register
EROMBRD	0x38	Expansion ROM Bus Region Description Register

You could also use the PCI - Base Address 1 I/O Mapped Configuration Registers.

7 Installation

7.1 I/O Circuit

The 64 I/O lines are realized with 8 x 74AHCT245 8 bit bus transceivers, a serial resistor and an array for ESD and overvoltage protection (see figure below “I/O Circuitry”). The maximum output current per line is +/- 8mA. There are no pull-up resistors, therefore unused inputs should be tied to Low or High.

Please note that the length of flat cables connected to the module should be kept very short to prevent large cross talk.

In the figure below only one I/O line is shown. There is one direction signal for each 8 bit port.

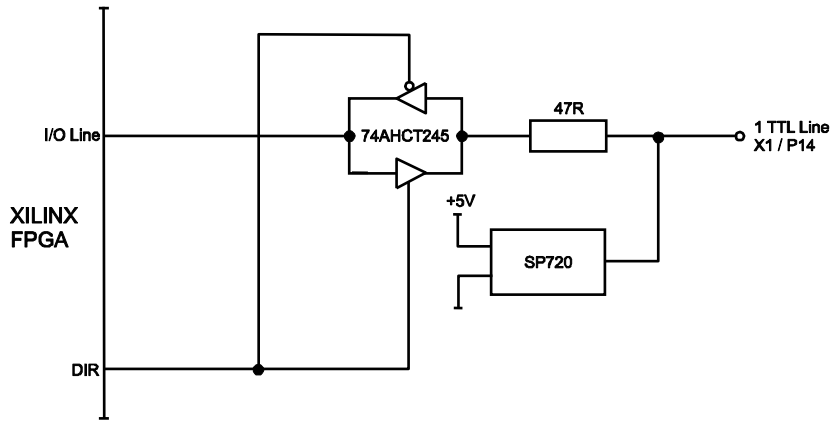

Table 7-1 : I/O Circuitry

7.2 Back I/O Configuration

The configuration of P14 64 pin Mezzanine “Back I/O” connector pins [57..64] can be changed between ground or port 2 [8..15] signals by zero ohm resistors.

For removing zero ohm resistors, work on a grounded, static free work surface.

The pads of the zero ohm resistors allow making a direct solder connection between the pads after removing the zero ohm resistors.

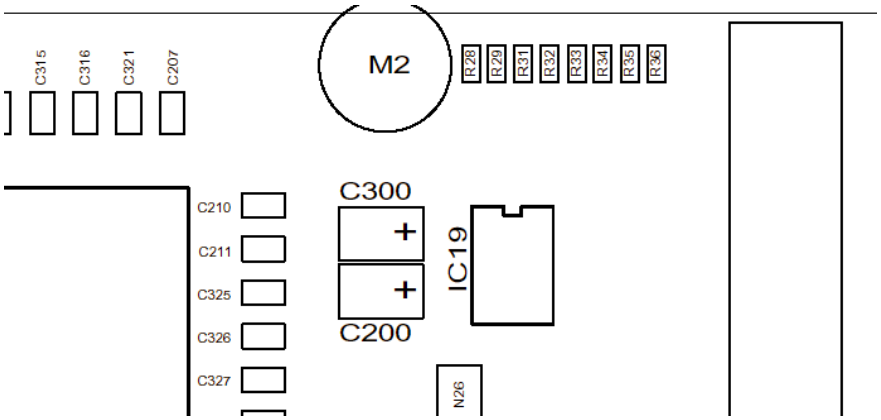

Figure 7-1 : Jumper positions for ground option

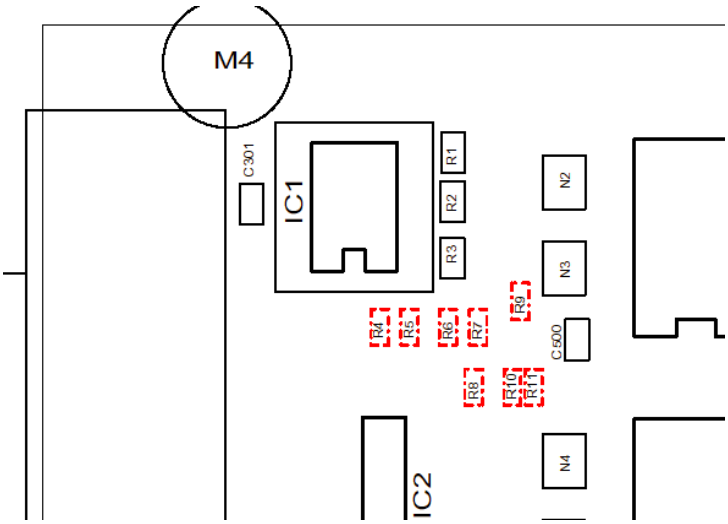

Figure 7-2 : Jumper positions for Port 2 signal option

Back I/O Pin	Signal	Jumper Position
57	ground (default)	R33
	Port 2 I/O Line 8	R8
58	ground (default)	R28
	Port 2 I/O Line 9	R9
59	ground (default)	R34
	Port 2 I/O Line 10	R10
60	ground (default)	R29
	Port 2 I/O Line 11	R11
61	ground (default)	R35
	Port 2 I/O Line 12	R7
62	ground (default)	R31
	Port 2 I/O Line 13	R6
63	ground (default)	R36
	Port 2 I/O Line 14	R5
64	ground (default)	R32
	Port 2 I/O Line 15	R4

Table 7-2 : Jumper positions for Back I/O options

Caution: Never make simultaneous connections on both jumper positions of one I/O line. Serious damage of the module is possible.

8 Pin Assignment – I/O Connector

8.1 Back I/O P14

See chapter "Back I/O Configuration".

Pin	Signal	Pin	Signal
1	Port 0, I/O Line 0	33	Port 4 I/O Line 0 (H1)
2	Port 0, I/O Line 1	34	Port 4 I/O Line 1 (H3)
3	Port 0, I/O Line 2	35	Port 4 I/O Line 2 (H5)
4	Port 0, I/O Line 3	36	Port 4 I/O Line 3
5	Port 0, I/O Line 4	37	Port 4 I/O Line 4
6	Port 0, I/O Line 5	38	Port 4 I/O Line 5
7	Port 0, I/O Line 6	39	Port 4 I/O Line 6
8	Port 0, I/O Line 7	40	Port 4 I/O Line 7
9	Port 0, I/O Line 8	41	Port 5 I/O Line 0 (H2)
10	Port 0, I/O Line 9	42	Port 5 I/O Line 1 (H4)
11	Port 0, I/O Line 10	43	Port 5 I/O Line 2 (H6)
12	Port 0, I/O Line 11	44	Port 5 I/O Line 3
13	Port 0, I/O Line 12	45	Port 5 I/O Line 4
14	Port 0, I/O Line 13	46	Port 5 I/O Line 5
15	Port 0, I/O Line 14	47	Port 5 I/O Line 6
16	Port 0, I/O Line 15	48	Port 5 I/O Line 7
17	Port 1, I/O Line 0	49	Port 2, I/O Line 0
18	Port 1, I/O Line 1	50	Port 2, I/O Line 1
19	Port 1, I/O Line 2	51	Port 2, I/O Line 2
20	Port 1, I/O Line 3	52	Port 2, I/O Line 3
21	Port 1, I/O Line 4	53	Port 2, I/O Line 4
22	Port 1, I/O Line 5	54	Port 2, I/O Line 5
23	Port 1, I/O Line 6	55	Port 2, I/O Line 6
24	Port 1, I/O Line 7	56	Port 2, I/O Line 7
25	Port 1, I/O Line 8	57	GND (Port 2, I/O Line 8)
26	Port 1, I/O Line 9	58	GND (Port 2, I/O Line 9)
27	Port 1, I/O Line 10	59	GND (Port 2, I/O Line 10)
28	Port 1, I/O Line 11	60	GND (Port 2, I/O Line 11)
29	Port 1, I/O Line 12	61	GND (Port 2, I/O Line 12)
30	Port 1, I/O Line 13	62	GND (Port 2, I/O Line 13)
31	Port 1, I/O Line 14	63	GND (Port 2, I/O Line 14)
32	Port 1, I/O Line 15	64	GND (Port 2, I/O Line 15)

Table 8-1 : P14 I/O Pin Assignment

Be sure that the P14 connector I/O signals are available and not otherwise used on the J14 connector of the PMC carrier board.

8.2 Front Panel I/O

All I/O ports are available on the HD68 SCSI 3-type front panel connector.

Pin	Signal	Pin	Signal
1	Port 0, I/O Line 0	35	Port 4 I/O Line 2 (H5)
2	Port 0, I/O Line 1	36	Port 4 I/O Line 3
3	Port 0, I/O Line 2	37	Port 4 I/O Line 4
4	Port 0, I/O Line 3	38	Port 4 I/O Line 5
5	Port 0, I/O Line 4	39	Port 4 I/O Line 6
6	Port 0, I/O Line 5	40	Port 4 I/O Line 7
7	Port 0, I/O Line 6	41	Port 5 I/O Line 0 (H2)
8	Port 0, I/O Line 7	42	Port 5 I/O Line 1 (H4)
9	Port 0, I/O Line 8	43	Port 5 I/O Line 2 (H6)
10	Port 0, I/O Line 9	44	Port 5 I/O Line 3
11	Port 0, I/O Line 10	45	Port 5 I/O Line 4
12	Port 0, I/O Line 11	46	Port 5 I/O Line 5
13	Port 0, I/O Line 12	47	Port 5 I/O Line 6
14	Port 0, I/O Line 13	48	Port 5 I/O Line 7
15	Port 0, I/O Line 14	49	Port 2, I/O Line 0
16	Port 0, I/O Line 15	50	Port 2, I/O Line 1
17	Port 1, I/O Line 0	51	Port 2, I/O Line 2
18	Port 1, I/O Line 1	52	Port 2, I/O Line 3
19	Port 1, I/O Line 2	53	Port 2, I/O Line 4
20	Port 1, I/O Line 3	54	Port 2, I/O Line 5
21	Port 1, I/O Line 4	55	Port 2, I/O Line 6
22	Port 1, I/O Line 5	56	Port 2, I/O Line 7
23	Port 1, I/O Line 6	57	Port 2, I/O Line 8
24	Port 1, I/O Line 7	58	Port 2, I/O Line 9
25	Port 1, I/O Line 8	59	Port 2, I/O Line 10
26	Port 1, I/O Line 9	60	Port 2, I/O Line 11
27	Port 1, I/O Line 10	61	Port 2, I/O Line 12
28	Port 1, I/O Line 11	62	Port 2, I/O Line 13
29	Port 1, I/O Line 12	63	Port 2, I/O Line 14
30	Port 1, I/O Line 13	64	Port 2, I/O Line 15
31	Port 1, I/O Line 14	65	GND
32	Port 1, I/O Line 15	66	GND
33	Port 4 I/O Line 0 (H1)	67	GND
34	Port 4 I/O Line 1 (H3)	68	GND

Table 8-2 : Front I/O Pin Assignment