The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC321

Conducion cooled 64 Digital TTL I/O / 32 Differential I/O

Version 1.0

User Manual

Issue 1.0.0

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TPMC321-10R

Conduction Cooled, 64-bit TTL I/O, Bit I/O, Interrupts, P14 I/O

(RoHS compliant)

TPMC321-11R

Conduction Cooled, 32-bit EIA-422 / EIA-485 I/O, Bit I/O, Interrupts, P14 I/O

(RoHS compliant)

TPMC321-12R

Conduction Cooled, 32-bit M-LVDS I/O, Bit I/O, Interrupts, P14 I/O

(RoHS compliant)

Issue	Description	Date
1.0.0	Initial issue	April 2022

Table of Contents

List of Figures

List of Tables

1 Product Description

The TPMC321 is a conduction cooled single-width 32 bit PMC module offering 64 ESD-protected 5V-tolerant TTL lines or 32 differential I/O lines using ESD-protected EIA-422 / EIA-485 compatible line transceivers or Multipoint-LVDS transceivers.

Each line is individually programmable as input, output or tri-state. The receivers are always enabled, which allows determining the state of each I/O line at any time. This can be used as read back function for lines configured as outputs. Each TTL I/O line has a pull-up resistor. The pull-up voltage is selectable to be either +3.3V or +5V. Differential I/O lines are terminated, EIA-422 / EIA-485 lines with 120 Ω, M-LVDS lines with 100 Ω.

Each input can generate an interrupt. Signal edge handling is programmable to interrupt on rising and/or falling edge of an input signal. Interrupts can be enabled and disabled for each bit. For interrupt source detection the status of each bit can be read from interrupt status registers.

The TPMC321 provides rear I/O via P14.

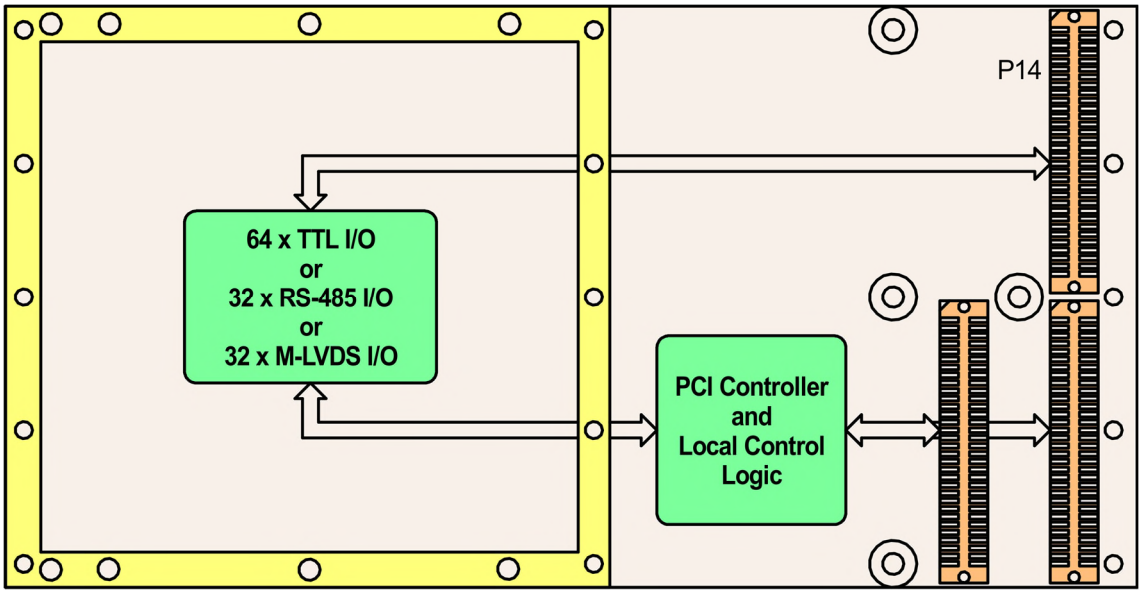

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface	
Mechanical Interface	Conduction Cooled PCI Mezzanine Card (PMC) Interface confirming to ANSI/VITA 20-2001 (R2005) Single Size (143.75 mm x 74 mm)
Electrical Interface	PCI Rev. 3.0 compatible 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage

On Board Devices	
PCI Target Chip and Local Control Logic	MachXO2 LCMXO2-4000HC (Lattice)
TTL Line Transceivers	74LVT126
EIA-485 Transceivers	MAX3078E
M-LVDS Transceivers	SN65MLVD206D

I/O Interface	
Number of Channels	64 TTL or 32 Differential Bit I/O Lines
I/O Standards	TTL signaling voltage level (maximum current: +/- 24 mA) EIA-485 with 120 Ω Termination M-LVDS with 100 Ω Termination
I/O Connector	PMC P14 I/O (64 pin Mezzanine Connector)

Physical Data		
Power Requirements	TPMC321-10R: 40 mA typical @ +5V (transceiver disabled, no load) 200 mA typical @ +5V (transceiver enabled, no load) TPMC321-11R: 50 mA typical @ +5V DC (transceiver disabled, no load) 700 mA typical @ +5V DC (transceiver enabled, no load)	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	TPMC321-10R: 350 000 h TPMC321-11R: 891 000 h TPMC321-12R: 845 000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	53 g	

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

This PMC module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done with appropriate care.

4 Terms and Definitions

4.1 Register Bit Access Types

Register Bit Access Type		Description
R	Read	The bit is readable by software
R/W	Read/Write	The bit is readable and writeable by software
R/C	Read/Clear	The bit is readable by software The bit is set by firmware Software may clear the bit by writing a '1'
R/S	Read/Set	The bit is readable by software Software may set this bit to '1' The bit is cleared by firmware

When reading reserved register bits, the read value is undefined.
For future software compatibility: For register write access reserved bits shall be written '0'.

4.2 Style Conventions

Hexadecimal characters are specified with prefix 0x (i.e. 0x029E).

For signals on hardware products, "Active Low" is represented by the signal name with an added # (i.e. IP_RESET#).

5 PCI Interface

5.1 PCI Identifiers

Vendor-ID	0x1498 (TEWS TECHNOLOGIES)
Device-ID	0x0141 (TPMC321)
Class Code	0x118000 (Other data acquisition/signal processing controllers)
Subsystem Vendor-ID	0x1498 (TEWS TECHNOLOGIES)
Subsystem Device-ID	0x000A (TPMC321-10R) 0x000B (TPMC321-11R) 0x000C (TPMC321-12R)

Table 5-1 : PCI Identifiers

5.2 PCI Base Address Register Configuration

For backward compatibility a subset of PCI9030 registers have been implemented within the PLD besides the Local Control Logic. This subset contains all registers that are used by the standard TEWS module driver.

PCI Base Address Register (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0 (0x10)	MEM	128	32	Little	Configuration Register Space
1 (0x14)	I/O	128	32	Little	
2 (0x18)	MEM	256	32	BIG *)	Functional Register Space

Table 5-2 : PCI Base Address Registers

*) Can be configured in the “Functional Register Space Descriptor (LAS0BRD)” register. Default is BIG.

5.3 Configuration Register Space

5.3.1 Register Map

Offset to PCI Base Address 2	Description	Size (Bit)
0x00 - 0x27	-	-
0x28	Local Address Space 0 Bus Region Descriptor (LAS0BRD)	32
0x2C - 0x4B	-	-
0x4C	Interrupt Control/Status (INTCSR)	32
0x50	Serial EEPROM and Initialization Control (CNTRL)	32
0x54	General Purpose I/O Control (GPIOC)	32
0x58 - 0x7B	-	-
0x7C	Configuration Space Revision Register (CREVREG)	32

Table 5-3 : Configuration Register Space

5.3.2 Register Description

5.3.2.1 Functional Register Space Descriptor (LAS0BRD)

Bit	Symbol	Description	Access	Reset Value
31:25	-	Reserved	R	0
24	ASBYTE_ORDER	Address Space Byte Ordering 1: activate Big Endian 0: activate Little Endian	R/W	1
23:0	-	Reserved	R	0

Table 5-4 : Functional Register Space Descriptor (LAS0BRD)

5.3.2.2 Interrupt Control/Status (INTCSR)

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved	R	0
7	SW_INT	Software Interrupt 1: generates PCI Interrupt (INTA# output asserted) if PCI Interrupt Enable bit is set (bit [6]=1) 0: clears PCI Interrupt	R/W	0
6	PCI_INT_EN	PCI Interrupt Enable 1: enables PCI interrupt 0: disables PCI interrupt	R/W	1
5:3	-	Reserved	R	0
2	LINT_STAT	Local Interrupt (LINTi1) Status 1: indicates interrupt active 0: indicates Interrupt not active	R	0
1	LINT_POL	Local Interrupt (LINTi1) Polarity 1: adjusts active high polarity 0: adjusts active low polarity	R/W	0
0	LINT_EN	Local Interrupt (LINTi1) Enable 1: enables Local Control Logic interrupts 0: disables Local Control Logic interrupts	R/W	1

Table 5-5 : Interrupt Control/Status (INTCSR)

5.3.2.3 Serial EEPROM and Initialization Control (CNTRL)

Bit	Symbol	Description	Access	Reset Value
31	-	Reserved	R	0
30	SWRST	Software Reset 1: resets the Functional Register Space. Reset stays active until it is cleared 0: clears the Functional Register Space reset	R/W	0
29	-	Reserved	R	0
28	EEPRSNT	Serial EEPROM Present 1: indicates serial EEPROM is present 0: indicates no serial EEPROM is present	R	1
27	EEDO	Serial EEPROM Data Out Bit This bit is the data output of the serial EEPROM	R	-
26	EEDI	Serial EEPROM Data In Bit This bit is the data input of the serial EEPROM	R/W	0
25	EECS	Serial EEPROM Chip Select 1: asserts serial EEPROM chip select 0: de-asserts serial EEPROM chip select	R/W	0
24	EESK	Serial EEPROM Clock Toggling this bit generates a serial EEPROM clock	R/W	0
23:0	-	Reserved	R	0

Table 5-6 : Serial EEPROM and Initialization Control (CNTRL)

5.3.2.4 General Purpose I/O Control (GPIOC)

Bit	Symbol	Description	Access	Reset Value
31:12	-	Reserved	R	0
11	GPIO3_DATA	GPIO3 Data Output Function: Stimulates corresponding pin Input Function: Provides state of corresponding pin	R/W	0
10	GPIO3_DDR	GPIO3 Data Direction 1: activates output function 0: activates input function	R/W	0
9	-	Reserved	R	0
8	GPIO2_DATA	GPIO2 Data Output Function: Stimulates corresponding pin Input Function: Provides state of corresponding pin	R/W	0
7	GPIO2_DDR	GPIO2 Data Direction 1: activates output function 0: activates input function	R/W	0
6	-	Reserved	R	0
5	GPIO1_DATA	GPIO1 Data Internally connected to 1 (backward compatibility). Formerly linked to PROGRAM# pin.	R/W	1
4	GPIO1_DDR	GPIO1 Data Direction GPIO1 represents PROGRAM# state. Hence the direction configuration is not implemented (input only).	R	0
3	-	Reserved	R	0
2	GPIO0_DATA	GPIO0 Data Internally connected to 1 (backward compatibility). Formerly linked to DONE pin.	R	1
1	GPIO0_DDR	GPIO0 Data Direction GPIO0 represents DONE state. Hence the direction configuration is not implemented (input only).	R	0
0	-	Reserved	R	0

Table 5-7 : General Purpose I/O Control (GPIOC)

The GPIO functionality has been implemented for backward-compatibility reason.

5.3.2.5 Configuration Space Revision Register (CREVREG)

Bit	Symbol	Description	Access	Reset Value
31:0	CREVREG	Firmware Version Register for Configuration Space	R	*)

Table 5-8 : Revision Register (CREVREG)

*) Depends on Firmware Version

5.4 Serial EEPROM

The serial EEPROM is not used for storing any configuration settings. All configuration data is stored within the internal Flash of the PLD. Hence, the device can be completely be used as memory.

For backward compatibility the serial EEPROM contains the configuration data of the previous version PCI controller.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x0141	0x1498	0x0280	0x0000	0x1180	0x0000	see below	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x0001	0x0000	0x0000
0x20	0x0000	0x0006	0x0000	0x0003	0x0FFF	0xFF00	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x1581	0x20A0	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0081	0x0000	0x0002	0x0000	0x0002
0x70	0x0000	0x0002	0x0030	0x0041	0x0078	0x0000	0x0000	0x0240
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 5-9: Serial EEPROM Content

Subsystem-ID Value (Offset 0x0C): TPMC321-10R: 0x000A

TPMC321-11R: 0x000B

TPMC321-12R: 0x000C

5.5 Functional Register Space

5.5.1 Register Map

Offset to PCI Base Address 2	Description	Size (Bit)
0x00	Output Register 0 (OUT_REG0)	32
0x04	Output Register 1 (OUT_REG1)	32
0x08	Input Register 0 (IN_REG0)	32
0x0C	Input Register 1 (IN_REG1)	32
0x10	Output Enable Register 0 (OE_REG0)	32
0x14	Output Enable Register 1 (OE_REG1)	32
0x18	Interrupt Status Register 0 (ISR0)	32
0x1C	Interrupt Status Register 1 (ISR1)	32
0x20	Positive Edge Interrupt Enable Register (PIER0)	32
0x24	Positive Edge Interrupt Enable Register (PIER1)	32
0x28	Negative Edge Interrupt Enable Register (NIER0)	32
0x2C	Negative Edge Interrupt Enable Register (NIER1)	32
0x30 - 0x7B	-	-
0xFC	Functional Register Space Revision Register (FREVREG)	32

Table 5-10 : Functional Register Space

5.5.2 Register Description

5.5.2.1 Output Register 0 (OUT_REG0)

Please note the “Output Line Switching”-chapter.

Bit	Symbol	Description	Access	Reset Value
31	OUT_REG_BIT_31	Output Port bit 31:0 Data	R/W	0
30	OUT_REG_BIT_30			
29	OUT_REG_BIT_29			
28	OUT_REG_BIT_28			
27	OUT_REG_BIT_27			
26	OUT_REG_BIT_26			
25	OUT_REG_BIT_25			
24	OUT_REG_BIT_24			
23	OUT_REG_BIT_23			
22	OUT_REG_BIT_22			
21	OUT_REG_BIT_21			
20	OUT_REG_BIT_20			
19	OUT_REG_BIT_19			
18	OUT_REG_BIT_18			
17	OUT_REG_BIT_17			
16	OUT_REG_BIT_16			
15	OUT_REG_BIT_15			
14	OUT_REG_BIT_14			
13	OUT_REG_BIT_13			
12	OUT_REG_BIT_12			
11	OUT_REG_BIT_11			
10	OUT_REG_BIT_10			
9	OUT_REG_BIT_9			
8	OUT_REG_BIT_8			
7	OUT_REG_BIT_7			
6	OUT_REG_BIT_6			
5	OUT_REG_BIT_5			
4	OUT_REG_BIT_4			
3	OUT_REG_BIT_3			
2	OUT_REG_BIT_2			
1	OUT_REG_BIT_1			
0	OUT_REG_BIT_0			

Table 5-11 : Output Register 0 (OUT_REG0)

5.5.2.2 Output Register 1 (OUT_REG1)

Please note the “Output Line Switching”-chapter. For the TPMC321-11R and -12R variants this register is read- and writeable, but the outputs are unused.

Bit	Symbol	Description	Access	Reset Value
63	OUT_REG_BIT_63	Output Port bit 63:32 Data	R/W	0
62	OUT_REG_BIT_62			
61	OUT_REG_BIT_61			
60	OUT_REG_BIT_60			
59	OUT_REG_BIT_59			
58	OUT_REG_BIT_58			
57	OUT_REG_BIT_57			
56	OUT_REG_BIT_56			
55	OUT_REG_BIT_55			
54	OUT_REG_BIT_54			
53	OUT_REG_BIT_53			
52	OUT_REG_BIT_52			
51	OUT_REG_BIT_51			
50	OUT_REG_BIT_50			
49	OUT_REG_BIT_49			
48	OUT_REG_BIT_48			
47	OUT_REG_BIT_47			
46	OUT_REG_BIT_46			
45	OUT_REG_BIT_45			
44	OUT_REG_BIT_44			
43	OUT_REG_BIT_43			
42	OUT_REG_BIT_42			
41	OUT_REG_BIT_41			
40	OUT_REG_BIT_40			
39	OUT_REG_BIT_39			
38	OUT_REG_BIT_38			
37	OUT_REG_BIT_37			
36	OUT_REG_BIT_36			
35	OUT_REG_BIT_35			
34	OUT_REG_BIT_34			
33	OUT_REG_BIT_33			
32	OUT_REG_BIT_32			

Table 5-12 : Output Register 1 (OUT_REG1)

5.5.2.3 Input Register 0 (IN_REG0)

Read directly from the I/O lines 31 to 0.

Bit	Symbol	Description	Access	Reset Value
31	IN_REG_BIT_31	Input Port bit 31:0 Data	R	-
30	IN_REG_BIT_30			
29	IN_REG_BIT_29			
28	IN_REG_BIT_28			
27	IN_REG_BIT_27			
26	IN_REG_BIT_26			
25	IN_REG_BIT_25			
24	IN_REG_BIT_24			
23	IN_REG_BIT_23			
22	IN_REG_BIT_22			
21	IN_REG_BIT_21			
20	IN_REG_BIT_20			
19	IN_REG_BIT_19			
18	IN_REG_BIT_18			
17	IN_REG_BIT_17			
16	IN_REG_BIT_16			
15	IN_REG_BIT_15			
14	IN_REG_BIT_14			
13	IN_REG_BIT_13			
12	IN_REG_BIT_12			
11	IN_REG_BIT_11			
10	IN_REG_BIT_10			
9	IN_REG_BIT_9			
8	IN_REG_BIT_8			
7	IN_REG_BIT_7			
6	IN_REG_BIT_6			
5	IN_REG_BIT_5			
4	IN_REG_BIT_4			
3	IN_REG_BIT_3			
2	IN_REG_BIT_2			
1	IN_REG_BIT_1			
0	IN_REG_BIT_0			

Table 5-13 : Input Register 0 (IN_REG0)

5.5.2.4 Input Register 1 (IN_REG1)

Read directly from the I/O lines 63 to 32. For the TPMC321-11R and -12R variants this register reads 0.

Bit	Symbol	Description	Access	Reset Value
63	IN_REG_BIT_63	Input Port bit 63:32 Data	R	-
62	IN_REG_BIT_62			
61	IN_REG_BIT_61			
60	IN_REG_BIT_60			
59	IN_REG_BIT_59			
58	IN_REG_BIT_58			
57	IN_REG_BIT_57			
56	IN_REG_BIT_56			
55	IN_REG_BIT_55			
54	IN_REG_BIT_54			
53	IN_REG_BIT_53			
52	IN_REG_BIT_52			
51	IN_REG_BIT_51			
50	IN_REG_BIT_50			
49	IN_REG_BIT_49			
48	IN_REG_BIT_48			
47	IN_REG_BIT_47			
46	IN_REG_BIT_46			
45	IN_REG_BIT_45			
44	IN_REG_BIT_44			
43	IN_REG_BIT_43			
42	IN_REG_BIT_42			
41	IN_REG_BIT_41			
40	IN_REG_BIT_40			
39	IN_REG_BIT_39			
38	IN_REG_BIT_38			
37	IN_REG_BIT_37			
36	IN_REG_BIT_36			
35	IN_REG_BIT_35			
34	IN_REG_BIT_34			
33	IN_REG_BIT_33			
32	IN_REG_BIT_32			

Table 5-14 : Input Register 1 (IN_REG1)

5.5.2.5 Output Enable Register 0 (OE_REG0)

Bit	Symbol	Description	Access	Reset Value
31	OE_REG_BIT_31	Output Enable bit 31:0 0: disables the output buffer 1: enables the output buffer	R/W	0
30	OE_REG_BIT_30			
29	OE_REG_BIT_29			
28	OE_REG_BIT_28			
27	OE_REG_BIT_27			
26	OE_REG_BIT_26			
25	OE_REG_BIT_25			
24	OE_REG_BIT_24			
23	OE_REG_BIT_23			
22	OE_REG_BIT_22			
21	OE_REG_BIT_21			
20	OE_REG_BIT_20			
19	OE_REG_BIT_19			
18	OE_REG_BIT_18			
17	OE_REG_BIT_17			
16	OE_REG_BIT_16			
15	OE_REG_BIT_15			
14	OE_REG_BIT_14			
13	OE_REG_BIT_13			
12	OE_REG_BIT_12			
11	OE_REG_BIT_11			
10	OE_REG_BIT_10			
9	OE_REG_BIT_9			
8	OE_REG_BIT_8			
7	OE_REG_BIT_7			
6	OE_REG_BIT_6			
5	OE_REG_BIT_5			
4	OE_REG_BIT_4			
3	OE_REG_BIT_3			
2	OE_REG_BIT_2			
1	OE_REG_BIT_1			
0	OE_REG_BIT_0			

Table 5-15: Output Enable Register 0 (OE_REG0)

5.5.2.6 Output Enable Register 1 (OE_REG1)

For the TPMC321-11R and -12R variants this register is read- and writeable, but the outputs are unused.

Bit	Symbol	Description	Access	Reset Value
63	OE_REG_BIT_63	Output Enable bit 63:32 0: disables the output buffer 1: enables the output buffer	R/W	0
62	OE_REG_BIT_62			
61	OE_REG_BIT_61			
60	OE_REG_BIT_60			
59	OE_REG_BIT_59			
58	OE_REG_BIT_58			
57	OE_REG_BIT_57			
56	OE_REG_BIT_56			
55	OE_REG_BIT_55			
54	OE_REG_BIT_54			
53	OE_REG_BIT_53			
52	OE_REG_BIT_52			
51	OE_REG_BIT_51			
50	OE_REG_BIT_50			
49	OE_REG_BIT_49			
48	OE_REG_BIT_48			
47	OE_REG_BIT_47			
46	OE_REG_BIT_46			
45	OE_REG_BIT_45			
44	OE_REG_BIT_44			
43	OE_REG_BIT_43			
42	OE_REG_BIT_42			
41	OE_REG_BIT_41			
40	OE_REG_BIT_40			
39	OE_REG_BIT_39			
38	OE_REG_BIT_38			
37	OE_REG_BIT_37			
36	OE_REG_BIT_36			
35	OE_REG_BIT_35			
34	OE_REG_BIT_34			
33	OE_REG_BIT_33			
32	OE_REG_BIT_32			

Table 5-16: Output Enable Register 1 (OE_REG1)

5.5.2.7 Interrupt Status Register 0 (ISR0)

The Interrupt Status Register signals the lines on which an interrupt event occurred. All interrupt sources are mapped to the local interrupt LINT1#. The local interrupt LINT1# is used in active low-level sensitive mode.

Bit	Symbol	Description	Access	Reset Value
31	INT_31	Line 31:0 Interrupt Request Status 0 = no active interrupt request 1 = active interrupt request Interrupts are acknowledged by writing '1' to the corresponding bit.	R/W	0
30	INT_30			
29	INT_29			
28	INT_28			
27	INT_27			
26	INT_26			
25	INT_25			
24	INT_24			
23	INT_23			
22	INT_22			
21	INT_21			
20	INT_20			
19	INT_19			
18	INT_18			
17	INT_17			
16	INT_16			
15	INT_15			
14	INT_14			
13	INT_13			
12	INT_12			
11	INT_11			
10	INT_10			
9	INT_9			
8	INT_8			
7	INT_7			
6	INT_6			
5	INT_5			
4	INT_4			
3	INT_3			
2	INT_2			
1	INT_1			
0	INT_0			

Table 5-17: Interrupt Status Register 0 (ISR0)

5.5.2.8 Interrupt Status Register 1 (ISR1)

The Interrupt Status Register signals the lines on which an interrupt event occurred. All interrupt sources are mapped to the local interrupt LINT1#. The local interrupt LINT1# is used in active low-level sensitive mode. For the TPMC321-11R and -12R variants this register reads 0.

Bit	Symbol	Description	Access	Reset Value
63	INT_63	Line 63:32 Interrupt Request Status 0 = no active interrupt request 1 = active interrupt request Interrupts are acknowledged by writing '1' to the corresponding bit.	R/W	0
62	INT_62			
61	INT_61			
60	INT_60			
59	INT_59			
58	INT_58			
57	INT_57			
56	INT_56			
55	INT_55			
54	INT_54			
53	INT_53			
52	INT_52			
51	INT_51			
50	INT_50			
49	INT_49			
48	INT_48			
47	INT_47			
46	INT_46			
45	INT_45			
44	INT_44			
43	INT_43			
42	INT_42			
41	INT_41			
40	INT_40			
39	INT_39			
38	INT_38			
37	INT_37			
36	INT_36			
35	INT_35			
34	INT_34			
33	INT_33			
32	INT_32			

Table 5-18: Interrupt Status Register 1 (ISR1)

5.5.2.9 Positive Edge Interrupt Enable Register 0 (PIER0)

Bit	Symbol	Description	Access	Reset Value
31	PIE_31	Line 31:0 Rising Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
30	PIE_30			
29	PIE_29			
28	PIE_28			
27	PIE_27			
26	PIE_26			
25	PIE_25			
24	PIE_24			
23	PIE_23			
22	PIE_22			
21	PIE_21			
20	PIE_20			
19	PIE_19			
18	PIE_18			
17	PIE_17			
16	PIE_16			
15	PIE_15			
14	PIE_14			
13	PIE_13			
12	PIE_12			
11	PIE_11			
10	PIE_10			
9	PIE_9			
8	PIE_8			
7	PIE_7			
6	PIE_6			
5	PIE_5			
4	PIE_4			
3	PIE_3			
2	PIE_2			
1	PIE_1			
0	PIE_0			

Table 5-19: Positive Edge Interrupt Enable Register 0 (PIER0)

5.5.2.10 Positive Edge Interrupt Enable Register 1 (PIER1)

For the TPMC321-11R and -12R variants this register is read- and writeable, but the interrupts are unused.

Bit	Symbol	Description	Access	Reset Value
63	PIE_63	Line 63:32 Rising Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
62	PIE_62			
61	PIE_61			
60	PIE_60			
59	PIE_59			
58	PIE_58			
57	PIE_57			
56	PIE_56			
55	PIE_55			
54	PIE_54			
53	PIE_53			
52	PIE_52			
51	PIE_51			
50	PIE_50			
49	PIE_49			
48	PIE_48			
47	PIE_47			
46	PIE_46			
45	PIE_45			
44	PIE_44			
43	PIE_43			
42	PIE_42			
41	PIE_41			
40	PIE_40			
39	PIE_39			
38	PIE_38			
37	PIE_37			
36	PIE_36			
35	PIE_35			
34	PIE_34			
33	PIE_33			
32	PIE_32			

Table 5-20: Positive Edge Interrupt Enable Register 1 (PIER1)

5.5.2.11 Negative Edge Interrupt Enable Register 0 (NIER0)

Bit	Symbol	Description	Access	Reset Value
31	NIE_31	Line 31:0 Falling Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
30	NIE_30			
29	NIE_29			
28	NIE_28			
27	NIE_27			
26	NIE_26			
25	NIE_25			
24	NIE_24			
23	NIE_23			
22	NIE_22			
21	NIE_21			
20	NIE_20			
19	NIE_19			
18	NIE_18			
17	NIE_17			
16	NIE_16			
15	NIE_15			
14	NIE_14			
13	NIE_13			
12	NIE_12			
11	NIE_11			
10	NIE_10			
9	NIE_9			
8	NIE_8			
7	NIE_7			
6	NIE_6			
5	NIE_5			
4	NIE_4			
3	NIE_3			
2	NIE_2			
1	NIE_1			
0	NIE_0			

Table 5-21: Negative Edge Interrupt Enable Register 0 (NIER0)

5.5.2.12 Negative Edge Interrupt Enable Register 1 (NIER1)

For the TPMC321-11R and -12R variants this register is read- and writeable, but the interrupts are unused.

Bit	Symbol	Description	Access	Reset Value
63	NIE_63	Line 63:32 Falling Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
62	NIE_62			
61	NIE_61			
60	NIE_60			
59	NIE_59			
58	NIE_58			
57	NIE_57			
56	NIE_56			
55	NIE_55			
54	NIE_54			
53	NIE_53			
52	NIE_52			
51	NIE_51			
50	NIE_50			
49	NIE_49			
48	NIE_48			
47	NIE_47			
46	NIE_46			
45	NIE_45			
44	NIE_44			
43	NIE_43			
42	NIE_42			
41	NIE_41			
40	NIE_40			
39	NIE_39			
38	NIE_38			
37	NIE_37			
36	NIE_36			
35	NIE_35			
34	NIE_34			
33	NIE_33			
32	NIE_32			

Table 5-22: Negative Edge Interrupt Enable Register 1 (NIER1)

5.5.2.13 Functional Space Revision Register (FREVREG)

Bit	Symbol	Description	Access	Reset Value
31:0	FREVREG	Firmware Version Register for Functional Space	R	*)

Table 5-23: Revision Register (FREVREG)

*) Depends on Firmware Version

6 Functional Description

6.1 TTL I/O Interface

Each of the 64 I/O lines is implemented with two 74LVT126 buffers as an interface to the FPGA pins. The logic levels of the buffers are TTL compatible, meaning that the minimum input high level is 2.0 V and the maximum input low level is 0.8 V. The nominal output high voltage is 3.3 V.

The buffer outputs are followed by 49.9 Ω serial resistors for signal integrity reasons. The 4.7 kΩ pull up resistors guaranty a high level when outputs are tristate and not driven externally.

In contrast to the buffer outputs, which must be explicitly enabled, the buffer inputs are permanently enabled.

As an option the pull up voltage can be set to 5V by jumper J1 to (weakly) drive a higher voltage than 3.3 V by setting the output to tristate. This means, instead of toggling the corresponding bit of the output register, the output enable register bit is set to 0 for an output high level or 1 to pull the output low (the OUT_REG bit is '0').

For example, when connecting to a standard 5 V CMOS logic input (not TTL compatible levels), a high level of minimum 3.5 V is required.

Please note that the pull up resistor can only drive high impedance inputs.

A TVS array protects against ESD shocks.

See the following figure for more information of the TTL I/O circuitry.

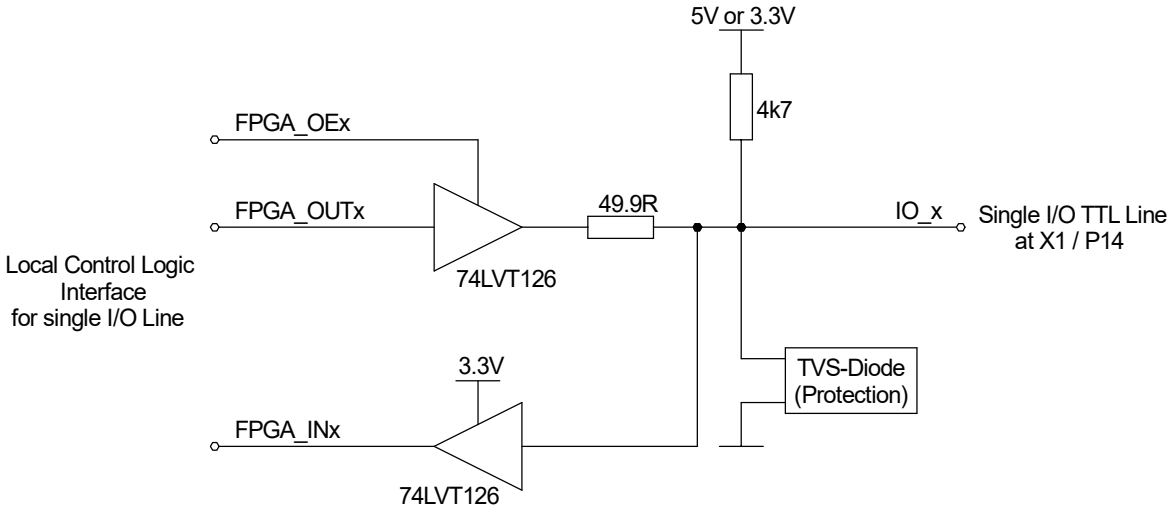

Figure 6-1 : TTL I/O Interface

6.1.1 Output Line Switching

Please note that the length (and consequently the capacitance) of a flat cable, connected to the TPMC321 module, should be kept as short as possible to prevent large cross talk.

To minimize crosstalk overshoots and ground bounce the output lines are switched in 8 groups of 8 signals with a delay of about 15 ns between 2 groups (@ 33 MHz PCI clock). This switching is done after every write access to Output or Output Enable Register.

6.1.2 TTL Buffer Pull Up Voltage

The voltage of the pull up resistors can be 3.3 V or alternatively 5 V, specified by jumper J1 for all I/O lines in common. The default pull up voltage is 3.3 V.

J1 Jumper Position	Pull Up Voltage
1 – 2	3.3 V (default)
2 – 3	5 V

Figure 6-2 : Pull Up Voltage Jumper Setting

6.2 Differential I/O-Interface

EIA-485 variants use 32 ESD-protected MAX3078E EIA-485/RS-422 transceivers and provide a 120 Ω termination resistors. LVDS variants use 32 ESD-protected SN65MLVD206 M-LVDS transceivers and provide a 100 Ω termination resistors.

The transceiver inputs are permanently enabled, transceiver outputs must be enabled through the Output Enable Register.

See the following figure for more information of the differential I/O circuitry.

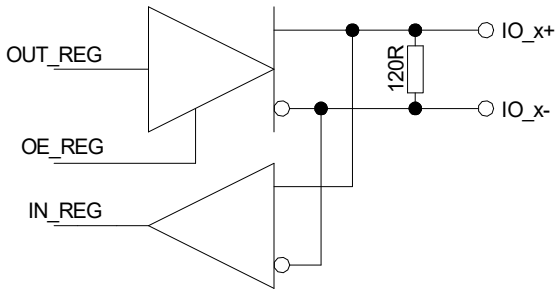

Figure 6-3 : Differential I/O Interface (EIA-422/485 Termination shown)

Please note that each differential I/O line provides its own termination. If more than two lines are connected together check carefully if the bus load is within allowed boundaries. If necessary, some termination resistor must be removed.

The actual data transmission rate depends on factors like connection, cable length, FPGA design etc.

6.3 Optional P14 Ground Connections

The configuration of P14 64 pin Mezzanine “Back I/O” connector lines [56:63] can be changed between I/O port signals (default) or ground connection by zero ohm resistors or solder bridges.

To change the connection from “I/O port” to “GND”, remove the zero ohm resistors on the top side of the PCB, and close the solder bridges on the bottom side of the PCB.

For removing zero ohm resistors, work on a grounded static free work surface.

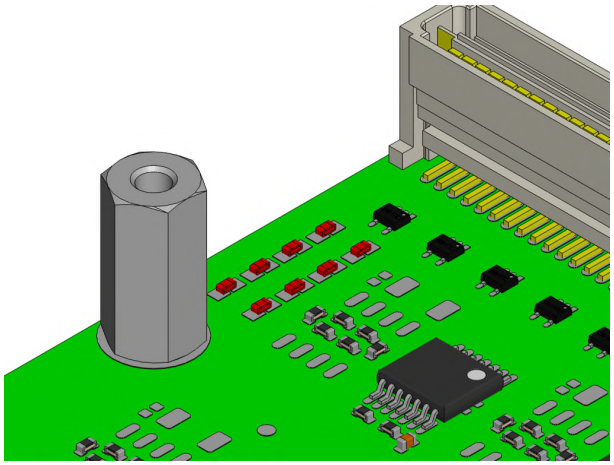

Figure 6-4 : Default 0Ω bridges on PCB top side (marked in red)

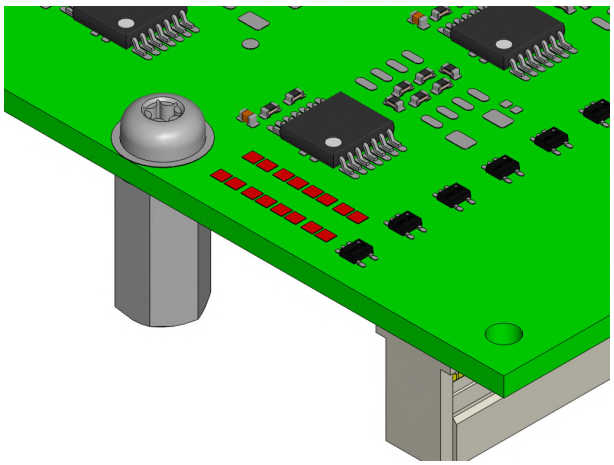

Figure 6-5 : Optional GND connection solder bridges on PCB bottom side (pads marked in red)

Caution: Never make simultaneous connections on both jumper positions of an I/O line. Serious damage of the module is possible.

7 Pin Assignment – I/O Connector

7.1 P14 Back I/O Connector

Pin	-10R	-11R	-12R
1	IO_0	IO_0-	IO_0-
2	IO_1	IO_0+	IO_0+
3	IO_2	IO_1-	IO_1-
4	IO_3	IO_1+	IO_1+
5	IO_4	IO_2-	IO_2-
6	IO_5	IO_2+	IO_2+
7	IO_6	IO_3-	IO_3-
8	IO_7	IO_3+	IO_3+
9	IO_8	IO_4-	IO_4-
10	IO_9	IO_4+	IO_4+
11	IO_10	IO_5-	IO_5-
12	IO_11	IO_5+	IO_5+
13	IO_12	IO_6-	IO_6-
14	IO_13	IO_6+	IO_6+
15	IO_14	IO_7-	IO_7-
16	IO_15	IO_7+	IO_7+
17	IO_16	IO_8-	IO_8-
18	IO_17	IO_8+	IO_8+
19	IO_18	IO_9-	IO_9-
20	IO_19	IO_9+	IO_9+
21	IO_20	IO_10-	IO_10-
22	IO_21	IO_10+	IO_10+
23	IO_22	IO_11-	IO_11-
24	IO_23	IO_11+	IO_11+
25	IO_24	IO_12-	IO_12-
26	IO_25	IO_12+	IO_12+
27	IO_26	IO_13-	IO_13-
28	IO_27	IO_13+	IO_13+
29	IO_28	IO_14-	IO_14-
30	IO_29	IO_14+	IO_14+
31	IO_30	IO_15-	IO_15-
32	IO_31	IO_15+	IO_15+

Pin	-10R	-11R	-12R
33	IO_32	IO_16-	IO_16-
34	IO_33	IO_16+	IO_16+
35	IO_34	IO_17-	IO_17-
36	IO_35	IO_17+	IO_17+
37	IO_36	IO_18-	IO_18-
38	IO_37	IO_18+	IO_18+
39	IO_38	IO_19-	IO_19-
40	IO_39	IO_19+	IO_19+
41	IO_40	IO_20-	IO_20-
42	IO_41	IO_20+	IO_20+
43	IO_42	IO_21-	IO_21-
44	IO_43	IO_21+	IO_21+
45	IO_44	IO_22-	IO_22-
46	IO_45	IO_22+	IO_22+
47	IO_46	IO_23-	IO_23-
48	IO_47	IO_23+	IO_23+
49	IO_48	IO_24-	IO_24-
50	IO_49	IO_24+	IO_24+
51	IO_50	IO_25-	IO_25-
52	IO_51	IO_25+	IO_25+
53	IO_52	IO_26-	IO_26-
54	IO_53	IO_26+	IO_26+
55	IO_54	IO_27-	IO_27-
56	IO_55	IO_27+	IO_27+
57 *)	IO_56	IO_28-	IO_28-
58 *)	IO_57	IO_28+	IO_28+
59 *)	IO_58	IO_29-	IO_29-
60 *)	IO_59	IO_29+	IO_29+
61 *)	IO_60	IO_30-	IO_30-
62 *)	IO_61	IO_30+	IO_30+
63 *)	IO_62	IO_31-	IO_31-
64 *)	IO_63	IO_31+	IO_31+

*) These pins allow an alternative ground connection, see “Optional P14 Ground Connections”

Table 7-1 : P14 Back I/O Connector