The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC151

4 Channel Resolver or LVDT/RVDT-to-Digital Converter

Version 1.0

User Manual

Issue 1.0.3

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TPMC151-10R

4 Channel Resolver or LVDT/RVDT-to-Digital Converter

(RoHS compliant)

TPMC151-20R

2 Channel Resolver or LVDT/RVDT-to-Digital Converter, 2 Channel Synchro-to-Digital Converter

(RoHS compliant)

Issue	Description	Date
1.0.0	Initial issue	January 2024
1.0.1	Added -20R variant	May 2024
1.0.2	Changed I/O connector to 50-pin MDR type	August 2024
1.0.3	- Added LOF CTRL bits to the Global Control Register to allow excitation input frequencies down to 400 Hz for all sensor types - Clarified ANGLE STROKE values for LVDT, and added “6.1 Transfer Function” for further clarification - Clarified the Combined Status Register Channel function - Clarified the valid Input Ranges for RDC / LVDT and Synchro - Clarified Ring Buffer function - Clarified BUF DONE, CLIP, LOS and QUAD interrupts	January 2025

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1 Product Description

The TPMC151 is a standard single-width 32-bit PMC module and supports a 33 MHz / 32-bit universal (5 V / 3.3 V) PCI interface.

The TPMC151-10R provides 4 channels of Resolver or LVDT/RVDT to Digital Converter with 16-bit resolution. It accepts input signals up to 12 V_{RMS}, with frequencies ranging from 1 kHz to 20 kHz and allows tracking rates up to ¼ of the excitation frequency (i.e. 10 kHz -> 2500 rps). The converter provides a digital angle, respectively stroke value, and a digital velocity value. For LVDT/RVDT differential and ratiometric sensor configuration is supported.

The TPMC151 provides individual excitation outputs with software selectable excitation frequency and output voltage swing for each channel. Adjustable frequency is ranging from 1 kHz to 20 kHz and the output voltage range is 0 to 12 V_{RMS} with up to 100 mA. No external power supply is required. Alternatively, an external excitation can be used.

The TPMC151-20R replaces two resolver channels with two Synchro-to-Digital Converter channels. For Synchro channels the excitation output is not available and an external excitation must be used. Synchro channels accept inputs signals up to 28 V_{RMS}, with frequencies ranging from 400 Hz to 20 kHz.

All TPMC151 signals are accessible through an 50-pin MDR type front I/O connector.

Software Support (TPMC151-SW-xx) for different operating systems is available.

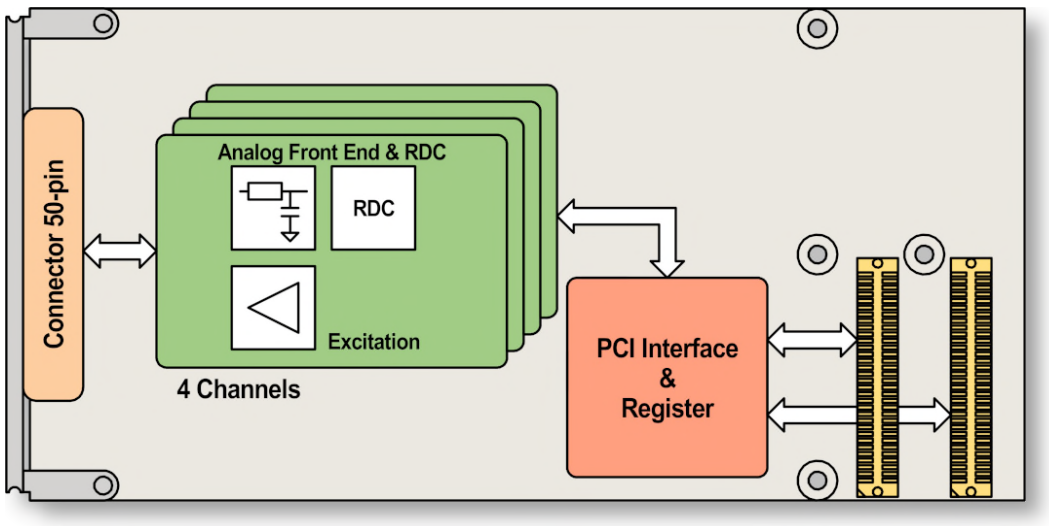

Figure 1-1 : Block Diagram TPMC151-10R

2 Technical Specification

PMC Interface	
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size (149 mm x 74 mm)
Electrical Interface	PCI Rev. 3.0 compliant 33 MHz / 32-bit PCI 3.3 V and 5 V PCI Signaling Voltage

On Board Devices	
PCI Target Chip	Artix-7 FPGA with PCI core
Analog Front End	AD7606C

I/O Interface	
Number of Channels	4
Supported Sensor Configuration	Resolver LVDT/RVDT: Differential (“4-wire”) and Ratiometric (“6-wire” or “5-wire”) Synchro (-20R only)
Excitation Output	0-12 V_{RMS}, up to 100 mA
Excitation Output Frequency	1-20 kHz
Excitation Input	RDC / LVDT Channels: 0-12 V_{RMS} Synchro Channels: 0-28 V_{RMS}
Excitation Input Frequency	RDC / LVDT Channels: 1-20 kHz Synchro Channels: 0.4-20 kHz
Sensor Input Voltage	RDC / LVDT Channels: 0-12 V_{RMS} Synchro Channels: 0-28 V_{RMS}
Resolution	Angle/Stroke: 16-Bit Velocity: 14-Bit
Tracking Rate	¼ Excitation Frequency
Accuracy	RDC: Up to 1.5 arcmin RDC Velocity: Up to ±0.5 % LVDT/RVDT: Up to ±0.06 % Synchro: Up to 4 arcmin

Physical Data		
Power Requirements	180 mA typical @ +5V (no load on Excitation Outputs) 600 mA @ +5V (All 4 EXC outputs driving 3 V_{RMS} @ 20 mA) 1800 mA @ +5V (All 4 EXC outputs driving 12 V_{RMS} @ 80 mA)	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	TPMC151-10R: 682000 h TPMC151-20R: 463000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	73 g	

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

This PMC module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done with appropriate care.

3.2 Power Dissipation

When using the excitation output, this PMC module requires adequate forced air cooling!

4 Terms and Definitions

4.1 Register Bit Access Types

Register Bit Access Type		Description
R	Read	The bit is readable by software
R/W	Read/Write	The bit is readable and writeable by software
R/C	Read/Clear	The bit is readable by software The bit is set by firmware Software may clear the bit by writing a '1'
R/S	Read/Set	The bit is readable by software Software may set this bit to '1' The bit is cleared by firmware

When reading reserved register bits, the read value is undefined.
For future software compatibility: For register write access, reserved bits shall be written '0'.

4.2 Style Conventions

Hexadecimal characters are specified with prefix 0x (i.e. 0x029E).

For signals on hardware products, "Active Low" is represented by the signal name with an added # (i.e. IP_RESET#).

4.3 Glossary

AFE Analog Front End

LVDT Linear Variable Differential Transformer

RDC Resolver to Digital Converter. Throughout this document "RDC" is used as "Resolver or LVDT/RVDT-to-Digital Converter"

RVDT Rotary Variable Differential Transformer. Since RVDTs works according to the same principle as LVDTs, through this document "LVDT" means "LVDT and/or RVDT"

5 PCI Interface

5.1 PCI Identifiers

Vendor-ID	0x1498 (TEWS Technologies)
Device-ID	0x0097 (TPMC151)
Class Code	0x118000 (Other data acquisition/signal processing controllers)
Subsystem Vendor-ID	0x1498 (TEWS Technologies)
Subsystem Device-ID	0x000A (TPMC151-10R) 0x0014 (TPMC151-20R)

Table 5-1 : PCI Identifiers

5.2 PCI Base Address Register Configuration

PCI Base Address Register (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0 (0x10)	MEM	512	32	Little	Internal Registers

Table 5-2 : PCI Base Address Registers

5.3 Internal Registers

Addresses and register bits marked as “reserved” should be written as ‘0’. Read values can be arbitrary and should not be relied upon.

5.3.1 Register Map

PCI Base Address Register 0 Offset	Description	Size (Bit)
0x000	Channel 1 Excitation Register	32
0x004	Channel 1 Data Register with Status	32
0x008	Channel 1 Data Register with Velocity	32
0x00C	Channel 1 Data Register with Sample Index	32
0x010-0x01C	Channel 2 (same as for Channel 1)	4x32
0x020-0x02C	Channel 3 (same as for Channel 1)	4x32
0x030-0x03C	Channel 4 (same as for Channel 1)	4x32
0x040	Combined Data Register 2 & 1	32
0x044	Combined Status Register 2 & 1	32
0x048	Combined Data Register 4 & 3	32
0x04C	Combined Status Register 4 & 3	32
0x050	AFE Control	32
0x054	AFE Status	32

PCI Base Address Register 0 Offset	Description	Size (Bit)
0x058	Input Range Register	32
0x05C-0x07C	reserved	-
0x80	Channel 1 Ring Buffer Control Register	32
0x84	Channel 1 Ring Buffer Status Register	32
0x88	Channel 1 Ring Buffer Data Register	32
0x8C	reserved	32
0x090-0x09C	Channel 2 (same as for Channel 1)	4x32
0x0A0-0x0AC	Channel 3 (same as for Channel 1)	4x32
0x0B0-0x0BC	Channel 4 (same as for Channel 1)	4x32
Global Registers		
0x0C0	Global Control Register	32
0x0C4	Status Register	32
0x0C8	Interrupt Enable Register	32
0x0CC	Interrupt Status Register	32
0x0D0-0x0DC	reserved	-
0x0E0	Interval Timer Control Register	32
0x0E4	Interval Timer Preload Register	32
0x0E8	Interval Timer Data Register	32
0x0EC	reserved	-
0x0F0	reserved	-
0x0F4	Board Health Register	32
0x0F8	Scratchpad Register	32
0x0FC	Firmware Version Register	32
0x100-0x1FC	reserved	-

Table 5-3 : Internal Registers

5.3.2 Register Description

Most registers described here are individual for each sensor. These are readily identifiable by a tailing “[x]”.

5.3.2.1 Channel [x] Excitation Register

Bit	Symbol	Description	Access	Reset Value
31:16	EXC FREQ	Excitation Frequency The Excitation Frequency on the x_EXC_OUT pins will be this value in Hz. Valid values are from 0x03E8 (= 1 kHz) to 0x4E20 (=20 kHz)	R/W	0x0000
15:8	EXC VOLT	Excitation Voltage The Excitation Voltage (the differential voltage between the [x]_EXC_OUT+ and [x]_EXC_OUT- pins) will be this value x 0,05 V_{RMS}. Useful values are from 0x28 (= 2 V_{RMS}) to 0xF0 (=12 V_{RMS})	R/W	0x00
7:1	-	Reserved	-	0
0	EXC ENA	Excitation Enable Set to ‘1’ to enable the Excitation. This enables the frequency generation and the output amplifier. This bit is automatically reset when AMP OT event was registered.	R/W	0

Table 5-4 : Channel [x] Excitation Register

5.3.2.2 Channel [x] Data Register with Status

The status bits in this register represent the actual status valid for the ANGLE STROKE value in this register. Status bits may be short-lived and volatile. To provide a way to catch intermittent states the “Status Register” provides mirrors of most of the status bits that are “sticky”, since they are latched until reset.

Bit	Symbol	Description	Access	Reset Value
31:25	-	Reserved, always reads as ‘0’	-	0
24	AMP OT	‘1’ = Excitation Output Overtemperature Flag The excitation amplifier signaled an overtemperature condition. This resets the EXC ENA bit in the “Channel [x] Excitation Register”, so the excitation output is disabled. This bit is cleared when the excitation is enabled again. Persisting overtemperature conditions will set this bit immediately back to ‘1’.	R	0
23	INIT DONE	‘1’ = RDC initialization done & output data is valid	R	0
22	LOF	‘1’ = RDC entered low frequency mode This bit is set when the Excitation frequency is lower than 4 kHz	R	0

Bit	Symbol	Description	Access	Reset Value
21	EXC HIGH	'1' = Excitation Frequency too high, f_{EXC} > 20 kHz If this bit is set while EXC LOW is also set, then the frequency is within limits, but not stable	R	0
20	EXC LOW	'1' = Excitation Frequency too low f_{EXC} < 400 Hz when LOF CTRLx is set to '1'or f_{EXC} < 1 kHz in all other modes. If this bit is set while EXC HIGH is also set, then the frequency is within limits, but not stable	R	0
19	CLIP COS	'1' = COS Clipping Clipping is position dependent While this bit is '1', neither the Angle/Stroke, nor the Velocity value are valid.	R	0
18	CLIP SIN	'1' = SIN Clipping Clipping is position dependent While this bit is '1', neither the Angle/Stroke, nor the Velocity value are valid.	R	0
17	LOS	'1' = SIN/COS Loss-of-Signal This bit is set when the sum of the SIN and COS signal is below 1/16 of the selected input range. I.e. with the 7,07 V_{RMS} input range selected this bit is set when the sum is below 0,44 V. This bit does not necessarily invalidate the Angle/Stroke or Velocity, but signals that performance may be degraded.	R	0
16	QUAD	'1' = Quadrant-Detection Error Possible causes are: - 180° jump - Excessive rotation speed - Excessive offsets - Excessive phase shifts (> 45°) While this bit is '1', neither the Angle/Stroke, nor the Velocity value are valid.	R	0
15:0	ANGLE STROKE	RDC & Synchro: Angle as unsigned value: LSB = $360°/2^{16}$ LVDT modes: Stroke as signed value: LSB = $\pm 100\%/2^{15}$ See "6.1 Transfer Function" for details	R	0

Table 5-5 : Channel [x] Data Register with Status

5.3.2.3 Channel [x] Data Register with Velocity

This register contains the angle or stroke value, with the velocity and the status bits that, when set, would invalidate the angle/stoke/velocity data.

Bit	Symbol	Description	Access	Reset Value
31	CLIP	SIN/COS Clipping An OR of the CLIP COS & CLIP SIN status bits in the "Channel [x] Data Register with Status"	R	0
30	QUAD	Quadrant-Detection Error As in "Channel [x] Data Register with Status"	R	0
29:16	VEL	Only valid for resolver Velocity Output in rps as signed value	R	0
15:0	ANGLE STROKE	RDC & Synchro: Angle as unsigned value: LSB = $360°/2^{16}$ LVDT modes: Stroke as signed value: LSB = $\pm 100\%/2^{15}$ See "6.1 Transfer Function" for details	R	0

Table 5-6 : Channel [x] Data Register with Velocity

5.3.2.4 Channel [x] Data Register with Sample Index

Bit	Symbol	Description	Access	Reset Value
31:16	SAMIDX	Sample count index, useful for time-based evaluation of data values, especially for LVDT sensors. SAMIDX is a counter that increments by 1 for each sample, and wraps around to zero after reaching the maximum value. The sample rate is 4.88 µs (or every 19.53 µs when in low frequency mode).	R	0
15:0	ANGLE STROKE	RDC & Synchro: Angle as unsigned value: LSB = $360°/2^{16}$ LVDT modes: Stroke as signed value: LSB = $\pm 100\%/2^{15}$ See "6.1 Transfer Function" for details	R	0

Table 5-7 : Channel [x] Data Register with Sample Index

5.3.2.5 Combined Data Register Channel 2 & 1 / 4 & 3

This register allows to read the data of two channels in a single access. This can be useful e.g. to read the angle of a multiturn resolver.

This register is available for Channel 2 & Channel 1 and for Channel 4 & Channel 3.

Bit	Symbol	Description	Access	Reset Value
31:16	ANGLE STROKE	RDC & Synchro: Angle as unsigned value: LSB = $360°/2^{16}$ LVDT modes: Stroke as signed value: LSB = $\pm 100\%/2^{15}$	R	0
15:0	ANGLE STROKE	RDC & Synchro: Angle as unsigned value: LSB = $360°/2^{16}$ LVDT modes: Stroke as signed value: LSB = $\pm 100\%/2^{15}$ See "6.1 Transfer Function" for details	R	0

Table 5-8 : Combined Data Register Channel 2 & 1 / 4 & 3

5.3.2.6 Combined Status Register Channel 2 & 1 / 4 & 3

This register allows to read the status of two channels in a single access. This can be useful e.g. to read the status of a multiturn resolver.

To ensure that a valid status for an associated Combined Data Register can be read, the status is latched when the Combined Data Register is read.

This register is available for Channel 2 & Channel 1 and for Channel 4 & Channel 3.

Bit	Symbol	Description	Access	Reset Value
31:16	STATUS	This is a latched mirror of the bits [31:16] of the “Output Register with Status” for Channel 2/4	R	0
15:0	STATUS	This is a latched mirror of the bits [31:16] of the “Output Register with Status” for Channel 1/3	R	0

Table 5-9 : Combined Status Register Channel 2 & 1 / 4 & 3

5.3.2.7 AFE Control Register

Analog Front End (AFE) Control Register.

Bit	Symbol	Description	Access	Reset Value
31:3	-	Reserved	-	0
2	AFE SET RANGE	Command: Set AFE Inputs Ranges Write ‘1’ to transfer the “Input Range Register” to the AFE. Conversions will continue, observe “AFE BUSY” in the “AFE Status Register” for completion of this command. Self-clearing bit, reads as ‘0’.	R/W	0
1	-	Reserved	-	0
0	AFE RESET	Software Reset Write ‘1’ to reset the AFE. This is a full reset to power-up default settings, including the AFE INIT. The reset status can be observed in the “AFE Status Register”. Self-clearing bit, reads as ‘0’.	R/W	0

Table 5-10 : AFE Control Register

5.3.2.8 AFE Status Register

Bit	Symbol	Description	Access	Reset Value
31:8	-	Reserved	-	0
2	AFE INIT	At startup the AFE initializes itself from a PROM. '1' = Initialization done, AFE is operational '0' = Initialization pending	R	0
1	AFE BUSY	AFE Access is in progress. At startup this bit indicates a running AFE initialization. After startup this bit indicates running "AFE Control Register" commands. Conversions are not interrupted, but allow this bit to return to '0' before issuing a new "AFE Control Register" command. '1' = AFE Initialization or AFE Access is in progress '0' = Idle, or converting	R	0
0	AFE DONE	Reset Done An AFE Reset is issued after startup, or through the AFE RESET bit in the "AFE Control Register". '1' = Reset Done '0' = Device Reset pending	R	0

Table 5-11 : AFE Status Register

5.3.2.9 Input Range Register

Use the values in this table for the Input Range setting:

Input Range [V_{RMS}]	Setting	Valid for
14.14 V_{RMS}	1011	RDC / LVDT
8.84 V_{RMS}	1010	
7.07 V_{RMS}	1001	
3.54 V_{RMS}	1000	
28 V_{RMS}	0011	TPMC151-20R Synchro-Channels
14 V_{RMS}	0001	
Reserved	All other	-

Table 5-12 : Input Ranges

The Input Ranges in the table are the maximum voltages for a given Input Range. The sensor voltage should be lower than that, to avoid clipping. Also refer to chapter “6. Functional Description” for further details how to setup the input range.

Use the “AFE SET RANGE” command in the “AFE Control Register” to make changes to this register active.

Changing the input range may result in step changes in the angle or stroke output data. Allow these changes to settle and check the status bits before using the angle or stroke output data.

The “RANGE SINx” and “RANGE COSx” setting of a channel must be set to the same Input Range. Synchro-Channels also use the SIN/COS range settings.

Bit	Symbol	Description	Access	Reset Value
31:28	RANGE COS4	Input Range for Channel 4 COS / Lb	R/W	1011
27:24	RANGE SIN4	Input Range for Channel 4 SIN / La	R/W	1011
23:20	RANGE COS3	Input Range for Channel 3 COS / Lb	R/W	1011
19:16	RANGE SIN3	Input Range for Channel 3 SIN / La	R/W	1011
15:12	RANGE COS2	Input Range for Channel 2 COS / Lb	R/W	1011
11:8	RANGE SIN2	Input Range for Channel 2 SIN / La	R/W	1011
7:4	RANGE COS1	Input Range for Channel 1 COS / Lb	R/W	1011
3:0	RANGE SIN1	Input Range for Channel 1 SIN / La	R/W	1011

Table 5-13 : Input Range Register

5.3.2.10 Channel [x] Ring Buffer Control Register

To support the measurement of singular events, the TPMC151 provides a triggerable “Ring Buffer” for each channel. When enabled, the ring buffer constantly records data values in the ring buffer. After crossing a programmable trigger value the buffer is filled up with the post trigger samples, then the recording of data values stops. After finishing the recording, the Ring Buffer can be read out. The Ring Buffer length is 4096 data samples, so read the “Channel [x] Ring Buffer Data Register” 4096 times, or as long as BUF AVAIL status bit is set.

A new sample is available every 4.88 µs (or every 19.53 µs when in low frequency mode). To increase the record length to a certain amount, a Data Divider is provided. The Data Divider only affects the recording, not the trigger detection. The ring buffer must be filled with at least PRE TRIG samples before a trigger is detected.

Disabling the Ring Buffer resets the internal pointers, but does not clear the Buffer itself. When the Ring Buffer is enabled, but BUF AVAIL is still ‘0’, it is possible to read old data. When reading data while BUF AVAIL is ‘0’, the data should be treated as stale.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:16</td><td>BUF TRIG</td><td>Ring Buffer Trigger Level
Crossing the Trigger Level starts the recording</td><td>R/W</td><td>0000</td></tr>
<tr><td>15:4</td><td>PRE TRIG</td><td>Pretrigger Count
Number of data values stored before the Trigger Level is crossed. The resulting number of Post-Trigger Samples is 4096 – PRE TRIG</td><td>R/W</td><td>0000</td></tr>
<tr><td>3:2</td><td>BUF DIV</td><td>Ring Buffer Data Divider
To increase the recording time, only the nth data value can be stored:
<table>
<tr><th>Div</th><th>Store</th><th>Recording Time</th></tr>
<tr><td>00</td><td>every value</td><td>20 ms</td></tr>
<tr><td>01</td><td>every 2nd value</td><td>40 ms</td></tr>
<tr><td>10</td><td>every 4th value</td><td>80 ms</td></tr>
<tr><td>11</td><td>every 8th value</td><td>160 ms</td></tr>
</table>
When in low frequency mode, the Recording Time is quadrupled.</td><td>R/W</td><td>00</td></tr>
<tr><td>1:0</td><td>BUF EDGE</td><td>Ring Buffer Trigger Edge Enable
The Ring Buffer can be triggered by low-to-high transitions through the Ring Buffer Trigger Level, or high-to-low transitions, or both:
<table>
<tr><th>Edge</th><th>Description</th></tr>
<tr><td>00</td><td>Ring Buffer disabled</td></tr>
<tr><td>01</td><td>Trigger by low-to-high transitions</td></tr>
<tr><td>10</td><td>Trigger by high-to-low transitions</td></tr>
<tr><td>11</td><td>Both</td></tr>
</table></td><td>R/W</td><td>00</td></tr>
</table>

Table 5-14 : Channel [x] Ring Buffer Control Register

5.3.2.11 Channel [x] Ring Buffer Status Register

Bit	Symbol	Description	Access	Reset Value
31:2	-	Reserved	-	-
1	BUF AVAIL	'1' = Data is available. Set when the recording has finished, reset when all data was read	R	0
0	BUF TRGD	'1' = Trigger event occurred, the Ring Buffer is filling with post trigger samples	R	0

Table 5-15 : Channel [x] Ring Buffer Status Register

5.3.2.12 Channel [x] Ring Buffer Data Register

The Ring Buffer contains the angle or stroke value, the velocity and the status bits that, when set, would invalidate the angle/stoke/velocity data. This is equivalent to the "Channel [x] Data Register with Velocity".

Bit	Symbol	Description	Access	Reset Value
31	CLIP	SIN/COS Clipping An OR of the CLIP COS & CLIP SIN status bits in the "Channel [x] Data Register with Status"	R	0
30	QUAD	Quadrant-Detection Error As in "Channel [x] Data Register with Status"	R	0
29:16	VEL	Velocity As in "Channel [x] Data Register with Velocity"	R	0
15:0	ANGLE STROKE	Resolver angle / LVDT stroke As in "Channel [x] Data Register"	R	0

Table 5-16 : Channel [x] Ring Buffer Data Register

5.3.2.13 Global Registers

5.3.2.13.1 Global Control Register

The channel mode is not only the selection of the sensor type, it also controls how the low frequency mode works. When the input excitation frequency is lower than 4 kHz, the TPMC151 automatically enters a low frequency mode. This is indicated by the “LOF” status bit.

The low frequency mode adapts internal filter times to the lower excitation frequency. In consequence, the reaction to angle and stroke changes is slower, and settling out step changes takes more time. When the LOF CTRLx is set to ‘1’, this time is increased to allow the use of excitation frequencies down to 400 Hz.

All modes behave the same for input excitation frequencies above 4 kHz. Only the channels with LOF CTRLx set to ‘1’ show the increased internal filter times in the low frequency mode. Please note that times given for the low frequency mode throughout this document must be further quadrupled when LOF CTRLx is set to ‘1’.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:16</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>15</td><td>LOF CTRL3</td><td>Low frequency mode control Channel 4
Same as below</td><td>R/W</td><td>0</td></tr>
<tr><td>14</td><td>-</td><td>reserved</td><td>-</td><td>-</td></tr>
<tr><td>13:12</td><td>MODE4</td><td>Mode Channel 4
Same as below</td><td>R/W</td><td>00</td></tr>
<tr><td>11</td><td>LOF CTRL3</td><td>Low frequency mode control Channel 3
Same as below</td><td>R/W</td><td>0</td></tr>
<tr><td>10</td><td>-</td><td>reserved</td><td>-</td><td>-</td></tr>
<tr><td>9:8</td><td>MODE3</td><td>Mode Channel 3
Same as below</td><td>R/W</td><td>00</td></tr>
<tr><td>7</td><td>LOF CTRL2</td><td>Low frequency mode control Channel 2
Same as below</td><td>R/W</td><td>0</td></tr>
<tr><td>6</td><td>-</td><td>reserved</td><td>-</td><td>-</td></tr>
<tr><td>5:4</td><td>MODE2</td><td>Mode Channel 2
Same as below</td><td>R/W</td><td>00</td></tr>
<tr><td>3</td><td>LOF CTRL1</td><td>Low frequency mode control Channel 1
‘0’ = Normal low frequency mode
‘1’ = Low frequency mode for excitations down to 400 Hz</td><td>R/W</td><td>0</td></tr>
<tr><td>2</td><td>-</td><td>reserved</td><td>-</td><td>-</td></tr>
<tr><td>1:0</td><td>MODE1</td><td>Mode Channel 1
<table>
<tr><th>Mode</th><th>Description</th></tr>
<tr><td>00</td><td rowspan="2">RDC
Also use this MODE for Synchros</td></tr>
<tr><td>01</td></tr>
<tr><td>10</td><td>Differential LVDT (A / B)</td></tr>
<tr><td>11</td><td>Ratiometric LVDT (A-B / A+B)</td></tr>
</table></td><td>R/W</td><td>00</td></tr>
</table>

Table 5-17 : Global Control Register

5.3.2.13.2 Status Register

This register provides a summary of the status bits in “Channel [x] Data Register with Status” from all four channels. It also latches the volatile status bits, allowing to catch intermediate error states. Latched bits are marked with a “R/C“ access and must be reset by writing a ‘1’ to the bit. The latched status bits in this register are used for interrupt generation. Latching is only done when the channel’s INIT DONE bit is set, so that error states during the initialization are inhibited, with the AMP OT bits as exception: An interrupt will be generated when the EXC ENA bit is reset due to an overtemperature condition signaled by the excitation amplifier.

Status bits that are set back to ‘1’ immediately after a clear indicate persisting status conditions.

Static status bits are marked with a “R” access and do not need to be reset.

Bit	Symbol	Description	Access	Reset Value
31:24	-	Status for Channel 4	-	0
23:16	-	Status for Channel 3	-	0
15:8	-	Status for Channel 2	-	0
7	INIT DONE (CH1)	‘1’ = RDC initialization done & output is valid	R	0
6	LOF (CH1)	‘1’ = RDC entered low frequency mode This bit is set when the Excitation frequency is lower than 4 kHz	R	0
5	EXC HIGH (CH1)	‘1’ = Excitation Frequency too high, f_{EXC} > 20 kHz	R	0
4	EXC LOW (CH1)	‘1’ = Excitation Frequency too low f_{EXC} < 400 Hz when LOF CTRLx is set to ‘1’ f_{EXC} < 1 kHz in all other modes.	R	0
3	AMP OT (CH1)	‘1’ = Excitation Output Overtemperature Flag The excitation amplifier signaled an overtemperature condition	R/C	0
2	CLIP (CH1)	‘1’ = A Clipping Error occurred This is an OR of the CLIP SIN and CLIP COS bits in the “Channel [x] Data Register with Status” register	R/C	0
1	LOS (CH1)	‘1’ = A Loss-of-Signal Error occurred This bit is set when the sum of the SIN and COS signal is below 1/16 of the selected input range. I.e. with the 7,07 V_{RMS} input range selected this bit is set when the sum is below 0,44 V. This bit does not necessarily invalidate the Angle/Stroke or Velocity, but signals that performance may be degraded.	R/C	0
0	QUAD (CH1)	‘1’ = A Quadrant-Detection Error occurred Possible causes are: - 180° jump - Excessive rotation speed - Excessive offsets - Excessive phase shifts (> 45°)	R/C	0

Table 5-18 : Status Register

5.3.2.13.3 Interrupt Enable Register

For pending interrupts and interrupt acknowledge see the Interrupt Status Register. Disabling an active interrupt removes the interrupt. It is recommended to enable the CLIP, LOS and QUAD interrupts only after the channel has the INIT DONE status.

Bit	Symbol	Description	Access	Reset Value
31	IRQ ACK CONF	Interrupt Acknowledge Configuration 0 = Interrupts are acknowledged by writing '1' to the appropriate bit in the "Interrupt Status Register" 1 = Interrupts are cleared when the "Interrupt Status Register" is read	R/W	0
30:21	-	Reserved, always reads as '0'	-	0
20	TIEN	Interval Timer Interrupt An interrupt is generated when the Interval Timer reaches zero	R/W	0
19	BUF DONE 4	Ring Buffer Data recording finished IRQ 1 = Ring Buffer Data Interrupt enabled 0 = Ring Buffer Data Interrupt disabled An interrupt will be generated when the recording has finished and BUF AVAIL is '1'.	R/W	0
18	BUF DONE 3		R/W	0
17	BUF DONE 2		R/W	0
16	BUF DONE 1		R/W	0
15	AMP OT 4	Excitation Amplifier Overtemperature IRQ 1 = Excitation Amplifier Overtemperature Interrupt enabled 0 = Excitation Amplifier Overtemperature Interrupt disabled An interrupt will be generated when the EXC ENA bit is reset due to an overtemperature condition signaled by the excitation amplifier.	R/W	0
14	AMP OT 3		R/W	0
13	AMP OT 2		R/W	0
12	AMP OT 1		R/W	0
11	CLIP 4	SIN/COS Clipping IRQ 1 = SIN/COS Clipping Interrupt enabled 0 = SIN/COS Clipping Interrupt disabled An interrupt will be generated when the CLIP bit in the "Channel [x] Data Register with status" is set to '1'.	R/W	0
10	CLIP 3		R/W	0
9	CLIP 2		R/W	0
8	CLIP 1		R/W	0
7	LOS 4	SIN/COS Loss-of-Signal IRQ 1 = Loss-of-Signal Interrupt enabled 0 = Loss-of-Signal Interrupt disabled An interrupt will be generated when the LOS bit in the "Channel [x] Data Register with status" is set to '1'.	R/W	0
6	LOS 3		R/W	0
5	LOS 2		R/W	0
4	LOS 1		R/W	0
3	QUAD 4	Quadrant-Detection Error IRQ 1 = Quadrant-Detection-Error Interrupt enabled 0 = Quadrant-Detection-Error Interrupt disabled An interrupt will be generated when the QUAD bit in the "Channel [x] Data Register with status" is set to '1'.	R/W	0
2	QUAD 3		R/W	0
1	QUAD 2		R/W	0
0	QUAD 1		R/W	0

Table 5-19 : Interrupt Enable Register

5.3.2.13.4 Interrupt Status Register

As above, just as status and with R/C access.

5.3.2.13.5 Interval Timer Control Register

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>31:3</td><td>-</td><td>Reserved, always reads as ‘0’</td><td>-</td><td>0</td></tr>
<tr><td>3</td><td>ITSET</td><td>Determines if the Interval Timer Clock Divider uses a prescaled clock or fixed time bases:
‘0’ = use prescaled clock
‘1’ = use time base</td><td>R/W</td><td>0</td></tr>
<tr><td>2:1</td><td>ITDIV</td><td>Interval Timer Clock Divider
Depending on ITSET the Interval Timer uses a prescaled clock or a fixed time base.
When using a prescaled clock:
<table>
<tr><th colspan="2">Value</th><th>Mode</th></tr>
<tr><td>0</td><td>0</td><td>10 MHz</td></tr>
<tr><td>0</td><td>1</td><td>5 MHz</td></tr>
<tr><td>1</td><td>0</td><td>2 MHz</td></tr>
<tr><td>1</td><td>1</td><td>1 MHz</td></tr>
</table>
When using a time base:
<table>
<tr><th colspan="2">Value</th><th>Mode</th></tr>
<tr><td>0</td><td>0</td><td>100 ns</td></tr>
<tr><td>0</td><td>1</td><td>1 µs</td></tr>
<tr><td>1</td><td>0</td><td>1 ms</td></tr>
<tr><td>1</td><td>1</td><td>1 s</td></tr>
</table></td><td>R/W</td><td>0</td></tr>
<tr><td>0</td><td>ITEN</td><td>Interval Timer Enable
'0' disables the Interval Timer
'1' enables the Interval Timer</td><td>R/W</td><td>0</td></tr>
</table>

Table 5-20 : Interval Timer Control Register

5.3.2.13.6 Interval Timer Preload Register

Bit	Symbol	Description	Access	Reset Value
31:0	ITPRE	Interval Timer Preload Register	R/W	0

Table 5-21 : Interval Timer Preload Register

5.3.2.13.7 Interval Timer Data Register

Bit	Symbol	Description	Access	Reset Value
31:0	ITDR	Interval Timer Data Register This register contains the actual Interval Timer Value.	R	0

Table 5-22 : Interval Timer Data Register

5.3.2.13.8 Board Health Register

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved	-	0
15:0	TEMP XADC	Result of the XADC on-chip temperature sensor measurement in degrees centigrade in steps of 1/256 °C. This is a signed value. A new readout is available every ~100 µs	R	0

Table 5-23 : Board Health Register

5.3.2.13.9 Scratchpad Register

Bit	Symbol	Description	Access	Reset Value
31:0	SCRATCH	Scratchpad Register Can be used to test read and write operations	R/W	0

Table 5-24 : Scratchpad Register

5.3.2.13.10 Firmware Identification Register

Bit	Symbol	Description	Access	Reset Value
31:24	FW_MAJ	Firmware Major Version	R	0x01
23:16	FW_MIN	Firmware Minor Version	R	0x00
15:8	FW_REV	Firmware Revision	R	x
7:0	FW_BLD	Firmware Build Count	R	x

Table 5-25 : Firmware Identification Register

6 Functional Description

6.1 Transfer Function

The ANGLE STROKE value represents an angle or a stroke value, depending on MODE setting for the channel.

For the MODE setting “00” & “01” (RDC & Synchro) the ANGLE STROKE value is a unsigned value, representing an angle as follows:

$$Angle\ in\ degrees = \frac{ANGLE\ STROKE \cdot 360°}{2^{16}}$$

$$Angle\ in\ minutes = \frac{ANGLE\ STROKE \cdot 21600'}{2^{16}}$$

$$Angle\ in\ radians = \frac{ANGLE\ STROKE \cdot 2\pi}{2^{16}}$$

For the MODE setting “10” & “11” (LVDT) the ANGLE STROKE value is a stroke value that can be positive or negative, so it is a signed value. A full stroke (positive or negative) is 100 %. With the MSB as sign, ANGLE STROKE represents a stroke value as follows:

$$Stroke\ in\ \% = \frac{ANGLE\ STROKE\ \cdot 100\%}{2^{15}}$$

6.2 Resolver

6.2.1 Resolver Wiring Modes

Wiring a resolver is straightforward. Choose your excitation source, and wire it according to the following diagrams:

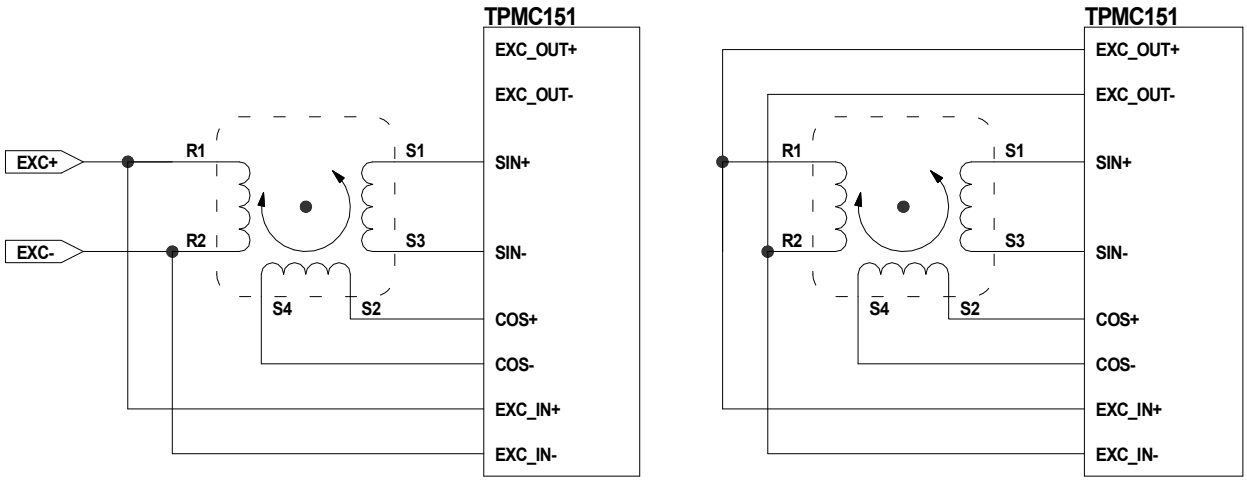

Figure 6-1 : Resolver Wiring with External and Internal Excitation

6.2.2 Design Procedure for Resolver

The key parameters for a resolver are the input voltage (or excitation voltage), the frequency of that voltage, and the transformation ratio, which determines the output voltage of the resolver.

Example resolver:

Parameter	Value
Excitation Voltage	2 V_{RMS} to 10 V_{RMS}, nominal 7 V_{RMS}
Excitation Frequency	4 kHz to 20 kHz, nominal 10 kHz
Transformation Ratio	0.5
Input Current	40 mA

Table 6-1 : Example Resolver Design Parameters

When using the internal excitation source the resolver input current must be smaller than the maximum current the TPMC151 can drive. In case the resolver input current exceeds 100 mA, an external excitation source must be used.

With the above resolver, using the nominal values, the TPMC151 would be set up as follows:

- Setup the excitation frequency & setup the excitation voltage: Set the “Channel [x] Excitation Register” to 0x2710_8C_01 to set the excitation frequency to 10 kHz, the excitation voltage to 7 V_{RMS} and to enable the excitation output.
- Set the input range. With the resolver's transformation ratio, the maximum input voltage would be 3.5 V_{RMS}, which is very close to the upper limit of the 3.54 V_{RMS} range. Hence, we set the input range to the 7.07 V_{RMS} range by writing “1001 for both the channel’s SIN and COS into the “Input Range Register”. Alternatively, the excitation voltage can be lowered a bit, to allow a bit more headroom for the input voltage, so the 3.54 V_{RMS} input range can be selected.

Resolver Input Voltages	Input Range Setting
3.54 V_{RMS}	1000
7.07 V_{RMS}	1001
8.84 V_{RMS}	1010
14.14 V_{RMS}	1011

Table 6-2 : Available Resolver Input Ranges

Observe the voltage and current limits of your Resolver, to avoid overloading the sensor, and potentially damaging it!

6.3 LVDT

6.3.1 LVDT Wiring Modes

The TPMC151 supports a differential and a ratiometric conversion for LVDTs. Both modes differ in wiring and in their basic conversion principle.

6.3.1.1 Differential Wiring

This wiring mode is often known as “4-wire LVDT”. It connects the LVDT’s secondary windings in series and measures the output over both secondaries. The other input of the converter is the excitation.

Differential Transfer Function: $Stroke = \frac{V_{A-B}}{V_{EXC}}$

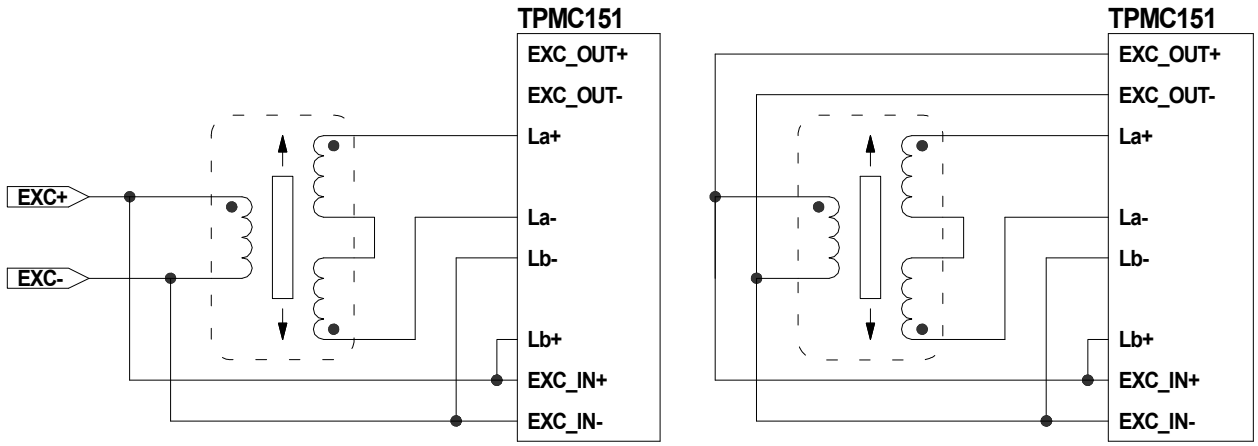

Figure 6-2 : LVDT Differential Wiring with External and Internal Excitation

6.3.1.2 Ratiometric Wiring

This wiring mode is often known as “6-wire LVDT”, or “5-wire LVDT”, the latter when the center tap is connected with only a single wire. In this wiring mode the secondary windings are measured separately.

Ratiometric Transfer Function: $Stroke = \frac{V_A - V_B}{V_A + V_B}$

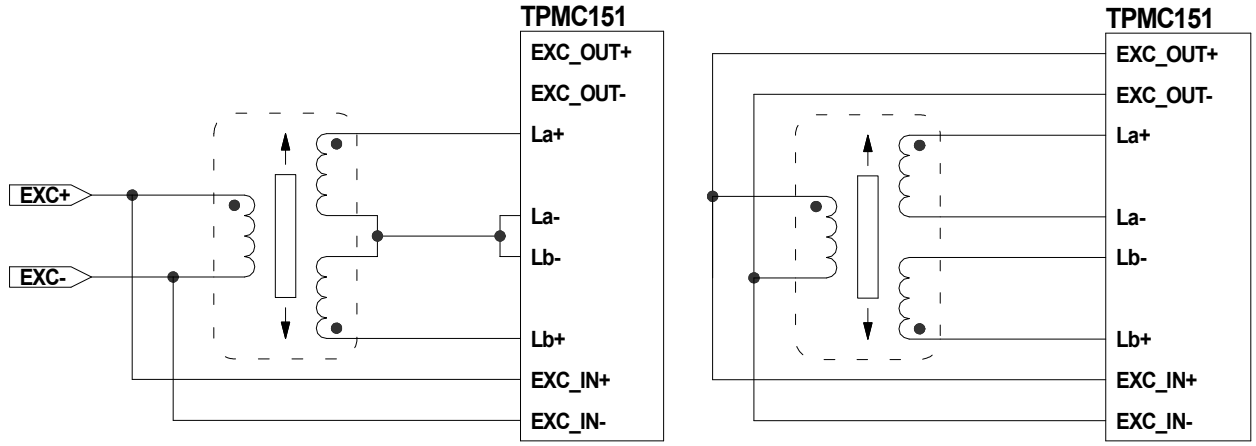

Figure 6-3 : LVDT 5-wire and 6-wire Ratiometric Wiring Examples

6.3.2 Design Procedure for LVDT

For the best possible performance of the TPMC151 in LVDT mode, it is important that the input voltage setting is carefully chosen together with the excitation voltage.

The key parameter for a LVDT is the sensitivity, which describes the output voltage depending on input voltage and stroke, and the stroke range. Another important parameter is the actually used stroke range.

If these parameters are unknown, then the setup can be done empirically. Set EXC voltage to the sensor's nominal value, connect the LVDT to the excitation and measure the La and Lb voltages at the maximum strokes. Then set an appropriate input range, or tweak the excitation voltage, so that the voltage at the maximum strokes fits nicely into the desired input range. Observe the sensor's voltage & current limits.

Otherwise calculate the full scale output for your sensor, using the desired excitation voltage (in V_{RMS}), the sensors sensitivity for the selected excitation frequency, and the full scale stroke:

$V_{FSO} = V_{EXC}$ x Sensitivity x Stroke

Using the ubiquitous E 100 as example, we get

V_{FSO} = 3 V_{RMS} x 94.5 mV/V/mm x 2.54 mm = 0.72 V_{RMS}

For a E 2000 we would get

V_{FSO} = 3 V_{RMS} x 18.1 mV/V/mm x 50.8 mm = 2.76 V_{RMS}

Now select a input range. Since the Input Ranges in the following table are "up to" voltages, the calculated V_{FSO} must be smaller than the selected Input Range:

Input Range [V_{RMS}]	Setting
14.14 V_{RMS}	1011
8.84 V_{RMS}	1010
7.07 V_{RMS}	1001
3.54 V_{RMS}	1000

Table 6-3 : Available LVDT Input Ranges

We would select the 3.54 V_{RMS} Input Range for both example sensors.

Observe the voltage and current limits of your LVDT, to avoid overloading the sensor, and potentially damaging it!

For best performance the Input Range should be utilized as much as possible. To give an example on how to archive this, we use an example LVDT with the following parameters:

Parameter	Value
Excitation Voltage	nominal 5 V_{RMS}, ±1 V_{RMS}
Excitation Frequency	50 Hz to 10 kHz, nominal 3 kHz
Stroke Range	±10 mm
Sensitivity	80 mV/V/mm

Table 6-4 : Example LVDT Design Parameters

Using the nominal parameters we get

V_{FSO} = 5 V_{RMS} x 80 mV/V/mm x 10 mm = 4 V_{RMS}

Which would fit in the 7.07 V_{RMS} Input Range. To utilize this range a bit more, we could rise the excitation to 6 V_{RMS}:

V_{FSO} = 6 V_{RMS} x 80 mV/V/mm x 10 mm = 4.8 V_{RMS}

Or we could lower the excitation to 4 V_{RMS}:

V_{FSO} = 4 V_{RMS} x 80 mV/V/mm x 10 mm = 3.2 V_{RMS}

and use the 3.54 V_{RMS} Input Range instead.

When we don't want to use the full nominal sensor stroke, i.e. to stay in the region with the best linearity, we can alter our calculation. Let's assume we want to use only 75% of the nominal stroke. Then we get:

V_{FSO} = 5 V_{RMS} x 80 mV/V/mm x 10 mm x 0.75 = 3 V_{RMS}

which would again fit nicely in the 3.54 V_{RMS} Input Range.

6.4 Synchro

Only for channel 3 & 4 of the TPMC151-20R.

6.4.1 Synchro Wiring Modes

Wiring a synchro is straightforward. Since the TPMC151 internal excitation cannot provide the usual synchro excitation voltage, only external excitation is possible. Wire it according to the following diagram:

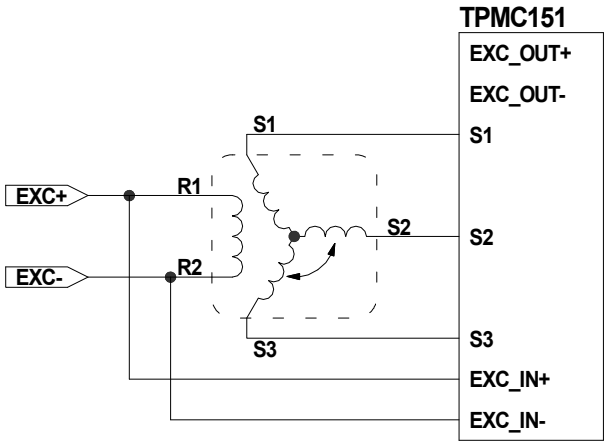

Figure 6-4 : Synchro Wiring with External Excitation

Observe the Maximum Voltage Ratings. Contact factory for a high voltage input option.

6.4.2 Design Procedure for Synchro

Use the RDC MODE setting for synchros.

Due to the voltage ratings of the typical cables and connectors, and limitations due to PCB layout, synchro voltages are limited to 30 V_{RMS}. For higher voltages a special variant that replaces the front I/O connector with a high-voltage adapter is necessary.

Synchros use special input range settings. Since the Input Ranges in the following table are “up to” voltages, the synchro voltage must be smaller than the selected Input Range:

Input Range [V_{RMS}]	Setting	Remark
28 V_{RMS}	0011	
14 V_{RMS}	0001	Use this range for an 11.8 V synchro

Table 6-5 : TPMC151-20R Synchro Input Ranges

6.5 Interval Timer

The interval timer is a 32-bit preloadable counter with a programmable clock rate. On activation the counter loads from the “Interval Timer Preload Register” und starts counting down. When the counter reaches zero, it generates an interrupt (if enabled), is automatically preloaded again and continues counting. The ITSET setting in the “Interval Timer Control Register” determines if the Interval Timer uses a prescaled clock or a time base.

Calculate the interval times using the prescaled clock with the following formula:

Interval Time = Value of “Interval Timer Preload Register” * Clock Period

ITDIV	Clock Frequency	Clock Period
00	10 MHz	100 ns
01	4 MHz	250 ns
10	2 MHz	500 ns
11	1 MHz	1 µs

Table 6-6 : Interval Timer Clock Periods

Calculate the interval times using the time base with the following formula:

Interval Time = Value of “Interval Timer Preload Register” * Time Base

ITDIV	Time Base
00	100 ns
01	1 µs
10	1 ms
11	1 s

Table 6-7 : Interval Timer Time Bases

The interval timer can be used as a reference timer in closed loop applications.

6.6 Ring Buffer

To support the measurement of singular events, the TPMC151 provides a triggerable “Ring Buffer” for each channel. When enabled, the ring buffer constantly records data values in the ring buffer. After crossing a programmable trigger value the buffer is filled up with the post trigger samples, then the recording of data values stops. After finishing the recording, the Ring Buffer can be read out. The Ring Buffer length is 4096 data samples, so read the “Channel [x] Ring Buffer Data Register” 4096 times, or as long as BUF AVAIL status bit is set.

A new sample is available every 4.88 µs (or every 19.53 µs when in low frequency mode). To increase the record length to a certain amount, a Data Divider is provided. The Data Divider only affects the recording, not the trigger detection. The ring buffer must be filled with at least PRE TRIG samples before a trigger is detected.

To reset the Ring Buffer, disable the Ring Buffer in the “Channel [x] Ring Buffer Control Register”.

The data stored in the Ring Buffer is equivalent to the “Channel [x] Data Register with Velocity”.

7 Pin Assignment – I/O Connector

7.1 Maximum Voltage Ratings

Pin Group	Example Signal	Maximum GND-related peak voltage per pin	Maximum Differential Voltage
Resolver & LVDT Input	1_SIN+, 1_LA+	±20 V	14 V_{RMS}
Excitation Input	1_EXC_IN+	±20 V	14 V_{RMS}
Excitation Output	1_EXC_OUT+	+22 V	15 V_{RMS}
Synchro Input	3_S1	+42 V	30 V_{RMS}
Synchro Excitation Input	3_SYN_EXC+	+42 V	30 V_{RMS}

Table 7-1 : Maximum Voltage Ratings

The EXC_OUT signals are not floating, but positive signals relative to ground, with a 11 V DC voltage when the Excitation Voltage is set to 0 V, and sinusoidal voltages between ground and 24 V when set to other voltages. The Excitation Voltage is the differential voltage between the EXC_OUT+ and EXC_OUT- pins.

7.2 Front Panel I/O Connector

Connector Type	HD 50 pos, female MDR type
Source & Order Info	3M# N10250-52E2PC (or compatible)

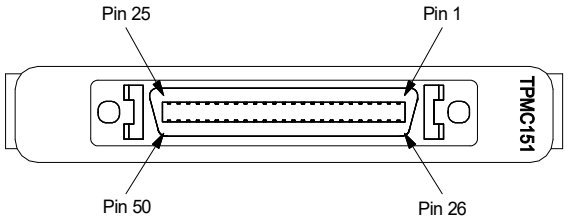

Figure 7-1 : Front Panel I/O Connector Pin Numbering

7.3 TPMC151-10R Front Panel I/O Pinout

Pin	Resolver	LVDT
1	1_SIN+	1_LA+
2	1_COS+	1_LB+
3	2_SIN+	2_LA+
4	2_COS+	2_LB+
5	3_SIN+	3_LA+
6	3_COS+	3_LB+
7	4_SIN+	4_LA+
8	4_COS+	4_LB+
9	1_EXC_IN+	
10	2_EXC_IN+	
11	3_EXC_IN+	
12	4_EXC_IN+	
13	AGND	AGND
14	1_EXC_OUT+	
15	2_EXC_OUT+	
16	3_EXC_OUT+	
17	4_EXC_OUT+	
18	-	-
19	-	-
20	-	-
21	-	-
22	-	-
23	-	-
24	-	-
25	-	-

Pin	Resolver	LVDT
26	1_SIN-	1_LA-
27	1_COS-	1_LB-
28	2_SIN-	2_LA-
29	2_COS-	2_LB-
30	3_SIN-	3_LA-
31	3_COS-	3_LB-
32	4_SIN-	4_LA-
33	4_COS-	4_LB-
34	1_EXC_IN-	
35	2_EXC_IN-	
36	3_EXC_IN-	
37	4_EXC_IN-	
38	AGND	AGND
39	1_EXC_OUT-	
40	2_EXC_OUT-	
41	3_EXC_OUT-	
42	4_EXC_OUT-	
43	-	-
44	-	-
45	-	-
46	-	-
47	-	-
48	-	-
49	-	-
50	-	-

Table 7-2 : TPMC151-10R Pin Assignment Front Panel I/O Connector

Since resolver and LVDTs are floating devices, the shown GND pins are not strictly necessary, but could be of use when the module is used with non-floating sensors or ground referenced equipment. Unused inputs can be left open.

Applications that use the excitation outputs must connect these externally to the excitation inputs.

The excitation outputs do not float, but are ground referenced. The EXC_OUT+/- signals are each positive voltages in reference to ground.

7.4 TPMC151-20R Front Panel I/O Pinout

With the synchro option the pins of the last two channels are not used, because these channels are occupied with the synchro conversion.

Pin	Resolver	LVDT
1	1_SIN+	1_LA+
2	1_COS+	1_LB+
3	2_SIN+	2_LA+
4	2_COS+	2_LB+
5	unused	
6	unused	
7	unused	
8	unused	
9	1_EXC_IN+	
10	2_EXC_IN+	
11	Unused	
12	Unused	
13	AGND	AGND
14	1_EXC_OUT+	
15	2_EXC_OUT+	
16	Unused	
17	Unused	
18	3_SYN_EXC_IN+	
19	4_SYN_EXC_IN+	
20	3_S1	
21	3_S2	
22	3_S3	
23	4_S1	
24	4_S2	
25	4_S3	

Pin	Resolver	LVDT
26	1_SIN-	1_LA-
27	1_COS-	1_LB-
28	2_SIN-	2_LA-
29	2_COS-	2_LB-
30	unused	
31	unused	
32	unused	
33	unused	
34	1_EXC_IN-	
35	2_EXC_IN-	
36	Unused	
37	Unused	
38	AGND	AGND
39	1_EXC_OUT-	
40	2_EXC_OUT-	
41	unused	
42	unused	
43	3_SYN_EXC_IN-	
44	4_SYN_EXC_IN-	
45	-	
46	-	
47	-	
48	-	
49	-	
50	-	

Table 7-3 : TPMC151-20R Pin Assignment Front Panel I/O Connector

Observe the Maximum Voltage Ratings for Synchros. Contact factory for a high voltage input option.

Since resolver, synchros and LVDTs are floating devices, the shown GND pins are not strictly necessary, but could be of use when the module is used with non-floating sensors or ground referenced equipment. Unused inputs can be left open.

Applications that use the excitation outputs must connect these externally to the excitation inputs.

The excitation outputs do not float, but are ground referenced. The EXC_OUT+/- signals are each positive voltages in reference to ground.