*The Embedded I/O Company*

TEWS TECHNOLOGIES

# TPCE240

## PCI Express x1, Mini PCIe Carrier Board

Version 1.0

## User Manual

Issue 1.0.0

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## TPCE240-10R

PCI Express x1 Carrier Board for one Mini PCIe Board



### Style Conventions

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. CLKREQ#.

# Document History

| Issue | Description | Date |
|---|---|---|
| 1.0.0 | Initial Issue | February 2025 |

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# 1 Product Description

The TPCE240 is a PCI Express Revision 2.0 compatible carrier board for one PCIe Mini Card. While specifically designed to run, test and maintain TEWS Mini PCI Express modules, it is an ideal solution for prototyping, but it can also be used to build modular, flexible and cost effective I/O solutions for all kinds of applications like process control, medical systems, telecommunication and traffic control.

Prototyping is facilitated by a couple of features: Clip latches allow to easily change the board without screws, a PCB cutout allows access to the PCIe Mini Cards from both sides, and a 12 V fan supply is provided for power demanding applications (if integrated on the mounted module). The supply source for the PCIe Mini Cards is selectable with a jumper setting (3.3 V PCIe, 3.3 V AUX or 12 V). The PCIe Mini Cards WxAN signals are connected to onboard LEDs.

A TEWS TA308 is partially integrated with providing the possible connection to an onboard JTAG Interface via XSR cable (XSR cable not included).

The TPCE240 also provides an option to adapt the PicoClasp connection usually used on TEWS PCIe Mini Cards to a MDR50 connector in the bracket (PicoClasp cable not included).

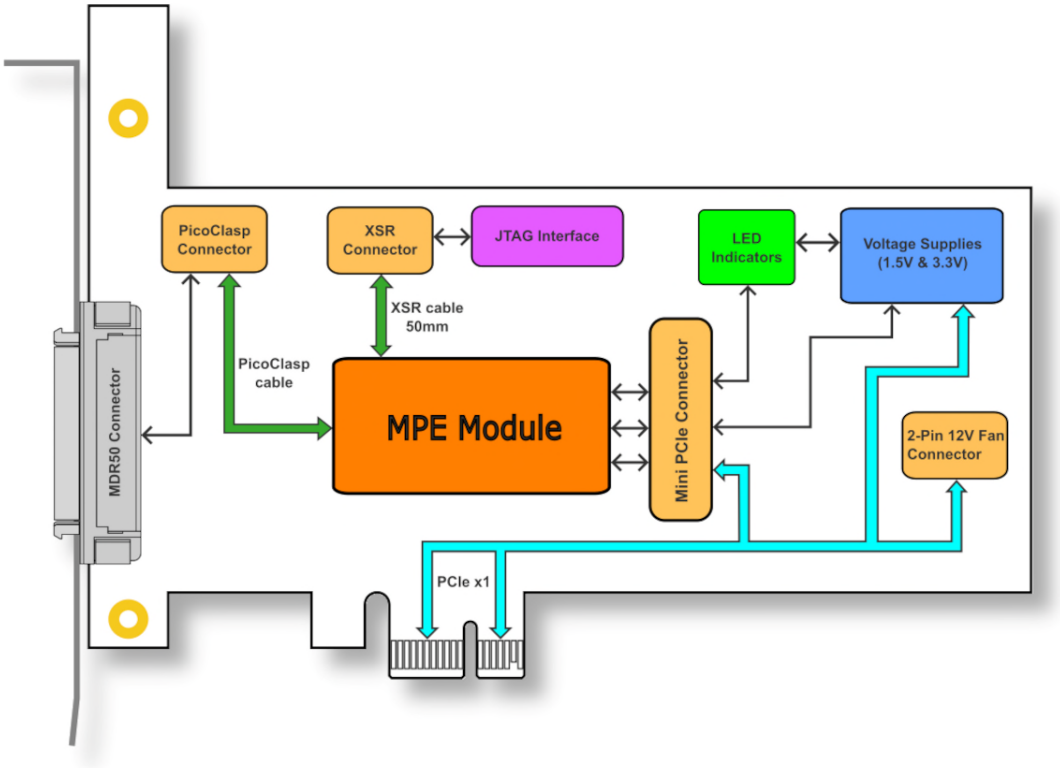



Figure 1-1 : Block Diagram

# 2 Technical Specification

| General | |
|---|---|
| **Mechanical Interface** | PCI Express x1, Revision 2.0 |
| **Electrical Interface** | PCI Express x1 Link conforming to PCIe Express Base Specification, Revision 2.0 |

| I/O Interface | |
|---|---|
| **I/O Connectors** | Front I/O:<br>50 pol Mini D Ribbon (MDR) Receptacle Connector (3M N10250-52E2PC or compatible) |

| Physical Data | |
|---|---|
| **Power Requirements** | 5 mA typical @ +12V DC (no module mounted) |
| **Available Slot Power** | 1.5 V: 3 A<br>3.3 V: 3 A (when supplied from 12 V, otherwise connected to backplane supply) |
| **Temperature Range** | Operating -40 °C to +85 °C<br>Storage -40 °C to +85 °C |
| **MTBF** | 716000 h<br>MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: $G_B$ 20°C.<br>The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation. |
| **Humidity** | 5 – 95 % non-condensing |
| **Weight** | 61.5 g |

Table 2-1 : Technical Specification

# 3 Handling and Operation Instructions

## 3.1 ESD Protection

**The TPCE240 is sensitive to static electricity. Packing, unpacking and all other handling of the TPCE240 has to be done in an ESD/EOS protected Area.**

# 4 Terms and Definitions

## 4.1 Style Conventions

"Active Low" signals are shown with a # suffix (i.e. RESET#).

# 5 Configuration Hints

## 5.1 Jumper Configuration

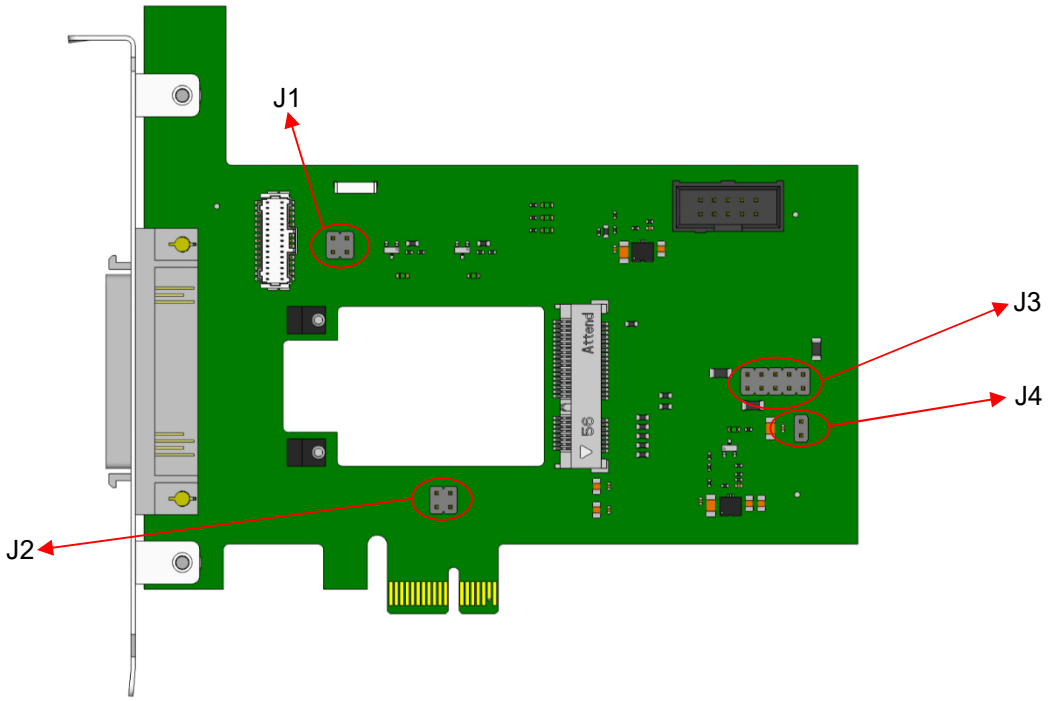



Figure 5-1 : Jumper Overview

Check descriptions below.

| Jumper | Pins | Function |
|---|---|---|
| J1 | 1 | GPIO0 XSR Connector |
| | 2 | GND |
| | 3 | GPIO1 XSR Connector |
| | 4 | GND |
| J2 | 1-2 | enables SMBus CLK |
| | 3-4 | enables SMBus Data |
| J3 | 1-2 | 3.3V Supply via 3.3V PCIe |
| | 3-4 | 3.3V Supply via 3.3Vaux PCIe |
| | 5-6 | 3.3V Supply via 3.3V Voltage Regulator |
| | 7-8 | n.c. |
| | 9-10 | GND |
| J4 | 1 | +12V |
| | 2 | GND |

Table 5-1 : Jumper Configuration

**J1:** The GPIO Pins of the debug interface are connected to a pin header for various use cases, for example indicating “PGOOD” and “FPGA done” or using it as a communication interface (UART).

**J2:** to connect the SMBus

**J3:** Jumperfield to choose which +3.3V voltage supply is used. In the diagram below it is shown in which way the selection works.

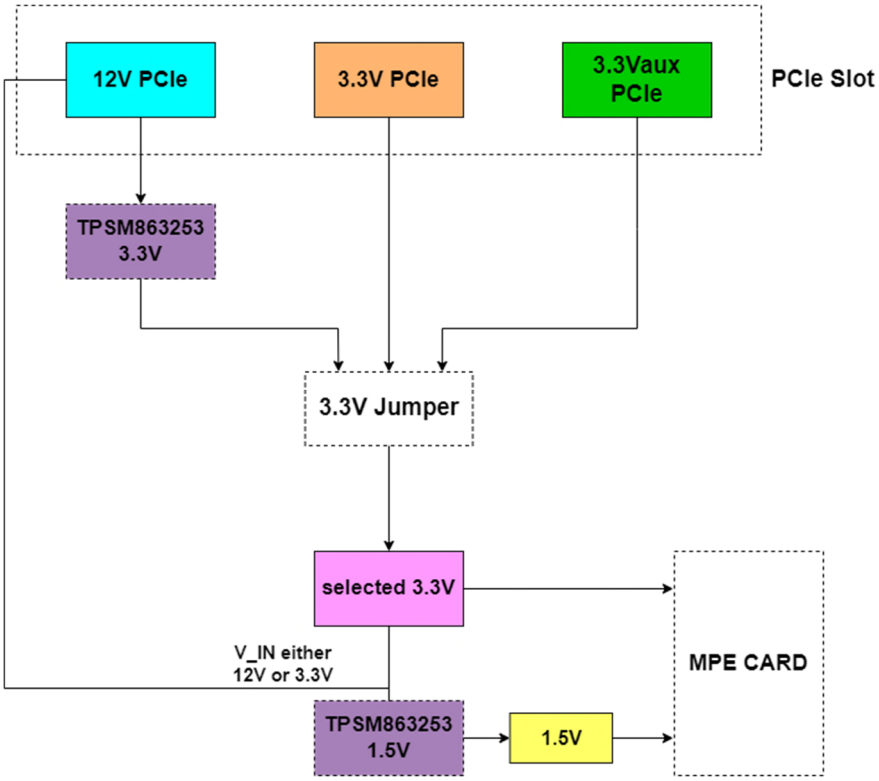



Figure 5-2 : +3.3V Selection Diagram

Three options to select 3.3V are onboard, the fourth is connecting external +3.3V. In that case connect +3.3V to Pin 1, 4 or 5 and GND to Pin 9 or 10. **Make sure to use only one out of four possibilities, otherwise it may cause damage to the board or peripherals.**

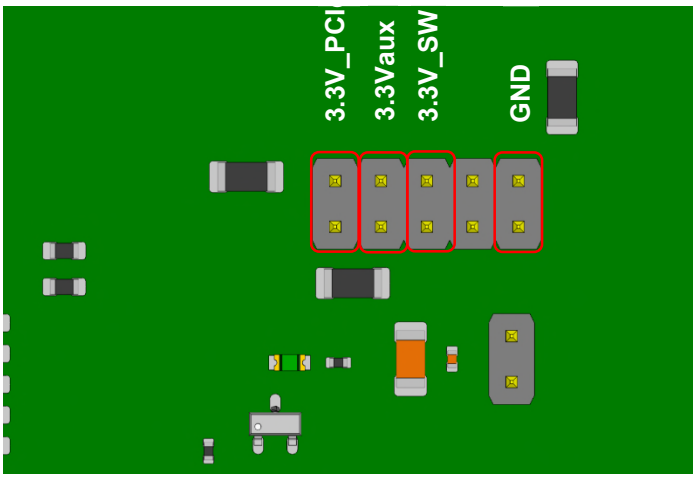



Figure 5-3 : +3.3V Jumper Configuration (J3)

**J4:** possibility to connect a fan for additional cooling

# 5.2 LED Description

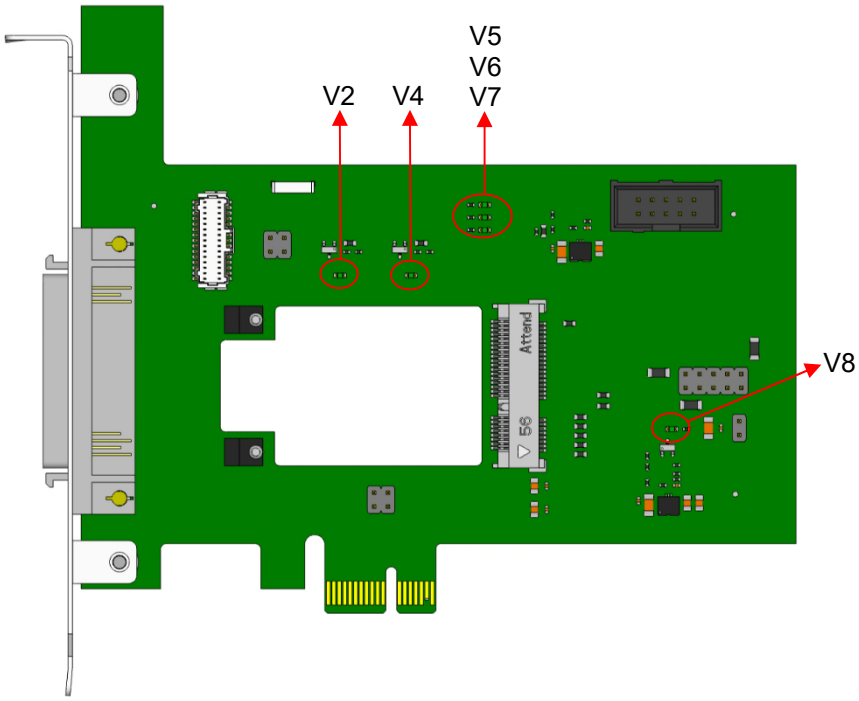



Figure 5-4 : LED Overview

| LED | Color | State | Description |
|---|---|---|---|
| V5 | Green | On | Mini PCIe WWAN Indication |
| | | Off | - |
| V6 | Green | On | Mini PCIe WLAN Indication |
| | | Off | - |
| V7 | Green | On | Mini PCIe WPAN Indication |
| | | Off | - |
| V4 | Green | On | GPIO1 XSR Connector Indication |
| | | Off | - |
| V2 | Green | On | GPIO0 XSR Connector Indication |
| | | Off | - |
| V8 | Green | On | 3.3V and 1.5V Supply are ok |
| | | Off | Supplies are not OK |

Table 5-2 : LED Description

# 5.3 Connector Overview

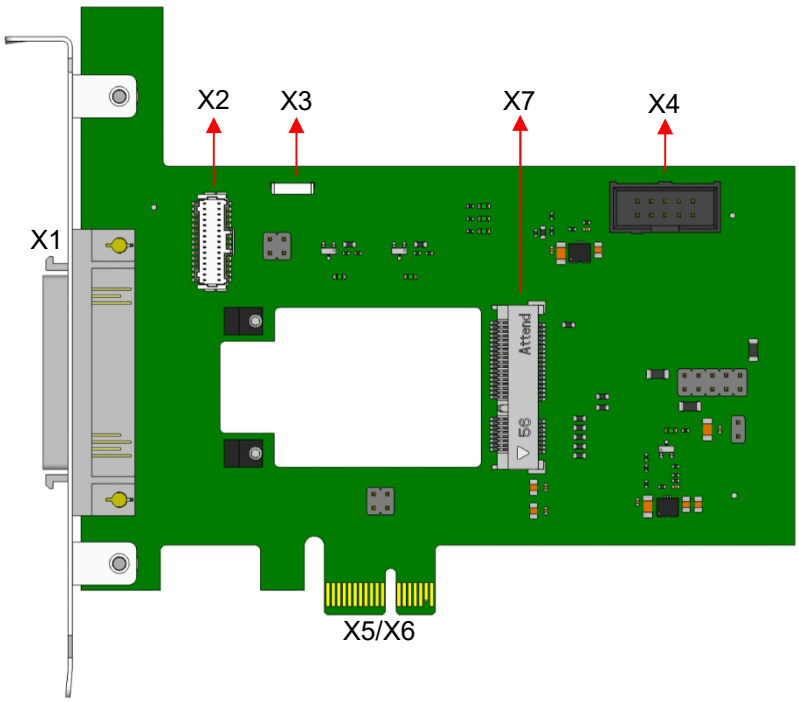



Figure 5-5 : Connector Overview

## 5.4 Front I/O Connector MDR50

Optional usage of the PicoClasp I/O signals of TEWS Mini PCIe Cards.

| | |
|---|---|
| **Pin-Count** | 50 |
| **Connector Type** | 50pol MDR |
| **Source & Order Info** | N10250-52E2PC, 3M Elec. Solutions (MDR) or compatible |

Table 5-3 : Front I/O MDR50

### 5.4.1 Pin Assignment

| Pin | Signal | Dir | Pin | Signal | Dir |
|---|---|---|---|---|---|
| 1 | I/O 1 | I/O | 26 | I/O 26 | I/O |
| 2 | I/O 2 | I/O | 27 | I/O 27 | I/O |
| 3 | I/O 3 | I/O | 28 | I/O 28 | I/O |
| 4 | I/O 4 | I/O | 29 | I/O 29 | I/O |
| 5 | I/O 5 | I/O | 30 | I/O 30 | I/O |
| 6 | I/O 6 | I/O | 31 | n.c. | - |
| 7 | I/O 7 | I/O | 32 | n.c. | - |
| 8 | I/O 8 | I/O | 33 | n.c. | - |
| 9 | I/O 9 | I/O | 34 | n.c. | - |
| 10 | I/O 10 | I/O | 35 | n.c. | - |
| 11 | I/O 11 | I/O | 36 | n.c. | - |
| 12 | I/O 12 | I/O | 37 | n.c. | - |
| 13 | I/O 13 | I/O | 38 | n.c. | - |
| 14 | I/O 14 | I/O | 39 | n.c. | - |
| 15 | I/O 15 | I/O | 40 | n.c. | - |
| 16 | I/O 16 | I/O | 41 | n.c. | - |
| 17 | I/O 17 | I/O | 42 | n.c. | - |
| 18 | I/O 18 | I/O | 43 | n.c. | - |
| 19 | I/O 19 | I/O | 44 | n.c. | - |
| 20 | I/O 20 | I/O | 45 | n.c. | - |
| 21 | I/O 21 | I/O | 46 | GND | - |
| 22 | I/O 22 | I/O | 47 | GND | - |
| 23 | I/O 23 | I/O | 48 | GND | - |
| 24 | I/O 24 | I/O | 49 | GND | - |
| 25 | I/O 25 | I/O | 50 | GND | - |

Table 5-4 : Front I/O Connector Pin Assignment

Direction and detailed signal descriptions depends on which Mini PCIe module is mounted on the carrier board. The MDR50 pinout is the same as the PicoClasp(X2) pinout of the mounted MPE module.

# 5.5 Onboard Connectors

## 5.5.1 x52 MPE

| | |
|---|---|
| **Pin-Count** | 52 |
| **Connector Type** | CONN PCI EXP MIN FML 52POS 0.031 |
| **Source & Order Info** | 119A-56A00-R02, Attend Technology or compatible |

Table 5-5 : x52 MPE

### 5.5.1.1 Pin Assignment

| Description | Connection | Pin | | Pin | Connection | Description |
|---|---|---|---|---|---|---|
| WAKE# | via 0R[2] | 1 | | 27 | GND | GND |
| 3.3V | 3.3V Jumper | 2 | | 28 | $V_{OUT}$ 1.5V regulator | 1.5V (1.5V/ANTCTRL0)[1] |
| COEX1 | via 0R to GND | 3 | | 29 | GND | GND |
| GND | GND | 4 | | 30 | pin header[2] | SMB_CLK |
| COEX2 | via 0R to GND | 5 | | 31 | direct[2] | PETn0 |
| 1.5V (1.5V/COEX3)[1] | $V_{OUT}$ 1.5V regulator | 6 | | 32 | pin header[2] | SMB_DATA |
| CLKREQ# | via 0R[2] | 7 | | 33 | direct[2] | PETp0 |
| UIM_PWR | n.c. | 8 | | 34 | GND | GND |
| GND | GND | 9 | | 35 | GND | GND |
| UIM_DATA | n.c. | 10 | | 36 | n.c. | USB_D- |
| REFCLK- | direct[2] | 11 | | 37 | GND | GND |
| UIM_CLK | n.c. | 12 | | 38 | n.c. | USB_D+ |
| REFCLK+ | direct[2] | 13 | | 39 | 3.3V Jumper | 3.3V |
| UIM_RESET | n.c. | 14 | | 40 | GND | GND |
| GND | GND | 15 | | 41 | 3.3V Jumper | 3.3V |
| UIM_SPU | n.c. | 16 | | 42 | onboard LED | LED_WWAN# |
| UIM_IC_DM | n.c. | 17 | | 43 | GND | GND |
| GND | GND | 18 | | 44 | onboard LED | LED_WLAN# |
| UIM_IC_DP | n.c. | 19 | | 45 | n.c. | ANTCTRL2 |
| W_DISABLE1# | via 0R to GND | 20 | | 46 | onboard LED | LED_WPAN# |
| GND | GND | 21 | | 47 | n.c. | ANTCTRL3 |
| PERST# | direct[2] | 22 | | 48 | $V_{OUT}$ 1.5V regulator | 1.5V (1.5V/ANTCTRL1)[1] |
| PERn0 | direct[2] | 23 | | 49 | n.c. | Reserved |
| 3.3V | 3.3V Jumper | 24 | | 50 | GND | GND |
| PERp0 | direct[2] | 25 | | 51 | via 0R to GND | W_DISABLE2# |
| GND | GND | 26 | | 52 | 3.3V Jumper | 3.3V |

Table 5-6 : x52 MPE Pin Assignment

[1]default pinout in brackets, red mark is used
[2]connected to PCIe Slot

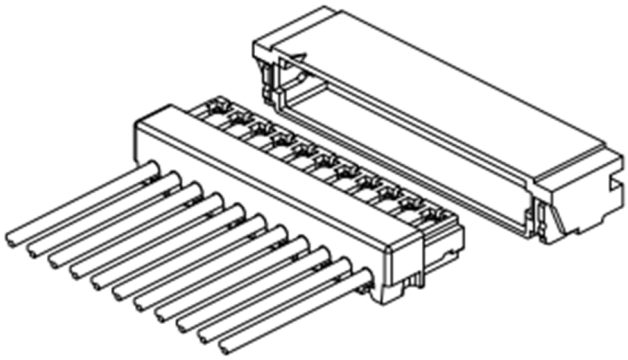
## 5.5.2 XSR x10

Optional connection to onboard JTAG Interface.

| | |
|---|---|
| **Pin-Count** | 10 |
| **Connector Type** | JST XSR 10pol 0,6 mm Pitch IDC Connector |
| **Source & Order Info** | SM10B-XSRS-ETB or compatible |

Table 5-7 : XSR x10

### 5.5.2.1 Pin Assignment



| Pin | Description |
|---|---|
| 1 | GND |
| 2 | TCK |
| 3 | TMS |
| 4 | TDI<br>(Test Data to MPE Card) |
| 5 | TDO<br>(Test Data from MPE Card) |
| 6 | GND |
| 7 | GPIO0 |
| 8 | GPIO1 |
| 9 | PRESENT1# |
| 10 | $V_{REF}$ |

Table 5-8 : XSR x10 Pin Assignment

## 5.5.3 BScan JTAG Connector

| | |
|---|---|
| **Pin-Count** | 10 |
| **Connector Type** | 10 pol, 2,54 mm header |
| **Source & Order Info** | 61201021621, Wurth Elektronik or compatible |

Table 5-9 : BScan JTAG Connector

### 5.5.3.1 Pin Assignment

| Description | Pin | | Pin | Description |
|---|---|---|---|---|
| PWR_CTRL# (opt.) | 10 |  | 9 | TRST# (opt.) |
| GND | 8 | | 7 | TDI |
| GND | 6 | | 5 | TDO (Test Data Driven by MPE Card) |
| GND | 4 | | 3 | TMS |
| GND | 2 | | 1 | TCK |

Table 5-10 : BScan JTAG Connector Pin Assignment

## 5.5.4 Jumper 3.3V

Jumper for selecting which 3.3V will be used.

| | |
|---|---|
| **Pin-Count** | 10 |
| **Connector Type** | 10 pol, 2,54 mm header |
| **Source & Order Info** | e.g. TSW-105-07-S-D, Samtec or compatible |

### 5.5.4.1 Pin Assignment

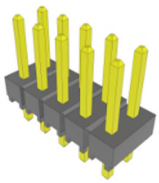
| Description | Pin | | Pin | Description |
|---|---|---|---|---|
| GND | 10 |  | 9 | GND |
| n.c. | 8 | | 7 | n.c. |
| $V_{OUT}$ 3.3V Regulator | 6 | | 5 | 3.3V x52 Connector |
| 3.3V x52 Connector | 4 | | 3 | 3.3Vaux PCIe Slot |
| 3.3V PCIe Slot | 2 | | 1 | 3.3V x52 Connector |

Table 5-11 : Jumper 3.3V Pin Assignment

## 5.5.5 Jumper XSR GPIO

| | |
|---|---|
| **Pin-Count** | 4 |
| **Connector Type** | 4 pol, 2,54 mm header |
| **Source & Order Info** | TSW-102-07-S-D-LL, Samtec or compatible |

Table 5-12 : Jumper XSR GPIO

### 5.5.5.1 Pin Assignment

| Description | Pin | | Pin | Description |
|---|---|---|---|---|
| GND | 4 |  | 3 | GPIO1 XSR Connector |
| GND | 2 | | 1 | GPIO0 XSR Connector |

Table 5-13 : Jumper XSR GPIO Pin Assignment

## 5.5.6 Jumper SMBus

Possible usage of the SMBus.

| | |
|---|---|
| **Pin-Count** | 4 |
| **Connector Type** | 4 pol, 2,54 mm header |
| **Source & Order Info** | TSW-102-07-S-D-LL, Samtec or compatible |

Table 5-14 : Jumper SMBus

### 5.5.6.1 Pin Assignment

| Description | Pin | | Pin | Description |
|---|---|---|---|---|
| SMB_DATA Mini PCIe | 4 |  | 3 | SMDAT PCIe Slot |
| SMB_CLK Mini PCIe | 2 | | 1 | SMCLK PCIe Slot |

Table 5-15 : Jumper SMBus Pin Assignment