The Embedded I/O Company

TEWS TECHNOLOGIES

TAMC200

Carrier for 3 IndustryPack®

Version 1.0

User Manual

Issue 1.0.2

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TAMC200-10R

AMC Carrier for 3 IndustryPack. Mid-size front panel ***)**

TAMC200-11R

AMC Carrier for 3 IndustryPack. Full-size front panel

***)** Please note that the mid-size module has restrictions to its usage because of a component height violation. It is within the responsibility of the user to carefully check if the mid-size module with its component height violation can be used in his system. Otherwise damage of the TAMC200 or its slot to be used in may occur!

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial Issue	July 2010
1.0.1	Corrected the Subsystem-ID entry in the PCI9030 PCI Configuration Header table (the actual Subsystem-ID has not been changed)	September 2011
1.0.2	(1) PCI9030 Local Space Endian Mapping changed to Little-Endian (to be compliant to other TEWS PCI based IP carriers). (2) Added information regarding FRU data Multi-Records	October 2011

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1 Product Description

The TAMC200 is a standard double mid-size or double full-size AMC.1 compliant carrier for up to three single-size (or one double-size and one single-size) IndustryPack (IP) modules, used to build modular, flexible and cost effective I/O solutions for all kinds of applications like process control, medical systems, telecommunication and traffic control. The TAMC200 is a versatile solution to upgrade well known legacy I/O solutions to a high performance form factor.

Three 68 pin SCSI-V (VHDCI/Champ) type connectors at the front panel provide access to all IP I/O lines.

All IP interrupt request lines are mapped to PCIe virtual wire interrupt messages. For fast interrupt source detection the TAMC200 provides an IP status register, including the interrupt status for all three IP slots.

The IP power lines are protected by resettable fuses and are RF filtered. Operating temperature range is -40°C to +85°C.

According to AMC.0, the TAMC200 provides an IPMI compliant Module Management Controller (MMC) with temperature monitoring and hot-swap support.

The TAMC200 is available as mid-size module or as full-size module. Please note that the mid-size module has restrictions to its usage because of a component height violation. It is within the responsibility of the user to carefully check if the mid-size module with its component height violation can be used in his system. Otherwise damage of the TAMC200 or its slot to be used in may occur!

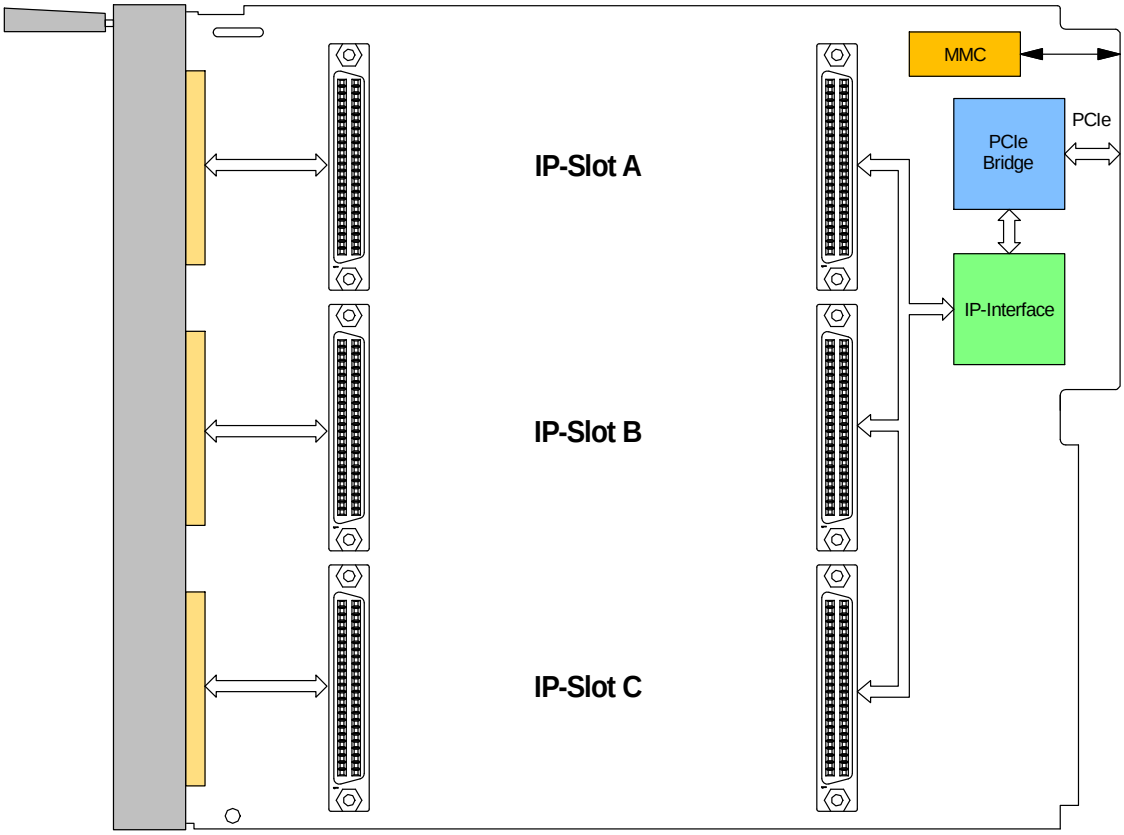

Figure 1-1 : Block Diagram

2 Technical Specification

AMC Interface			
Mechanical Interface	Advanced Mezzanine Card (AMC) Interface confirming to PICMG® AMC.0 R2.0 Single, Mid / Full Size Module		
Electrical Interface	PICMG® AMC.1 R1.0 PCIe single lane (x1) port (AMC.1 Type 1 compliant)		
IPMI			
IPMI Version	1.5		
Front Panel LEDs (MMC controlled)	Blue Hot-Swap LED, Red Out-Of-Service/Failure LED (LED1), Green OK/Activity LED (LED 2)		
On Board Devices			
PCI Express / PCI Bridge	PEX8112 (PLX Technology)		
PCI Target Chip	PCI9030 (PLX Technology)		
IP FPGA	XC2S50 (Xilinx)		
IP Interface			
IP Interface	According to IndustryPack specification ANSI / VITA 4-1995 8 / 16 bit access 8 / 32 MHz selectable per IP slot 8 MByte memory space per IP slot TTL Level		
IP Slots	Three single-size IP slots (A, B, C). IP Slots A+B may be used for a double-size IP Module		
Mapping of IP Interrupts	Routing of all IP interrupts to PCIe INTA/MSI. Local interrupt status register		
DMA	Not supported		
32-Bit Access	Not supported in the current implementation		
Power Supply	Resettable fuses and RF-filtering on all IP power lines		
I/O Interface			
I/O Connector	Front-I/O via 68 pin SCSI-V (VHDCI/Champ) type connector per IP slot		
IP LEDs	One LED per IP slot. Indicates IP module activity (LED flashes on when the IP module generates the acknowledge signal)		
Physical Data			
Power Requirements	0.3A typical @ +12V DC (Payload Power) 42mA typical @ +3.3V DC (Management Power) (without any IP module plugged. IP modules require additional power)		
Temperature Range	Operating Storage	-40°C - +85°C -40°C - +85°C	
MTBF	250.000 h		

	MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	185 g

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

The TAMC200 is sensitive to Electrostatic Discharge (ESD).
Packing, unpacking and all other handling of the TAMC200 has to be done in an ESD/EOS protected Area.

3.2 TAMC200 Mid-size Option Usage Restrictions

Please note that the mid-size module has restrictions to its usage because of a component height violation. It is within the responsibility of the user to carefully check if the mid-size module with its component height violation can be used in his system. Otherwise damage of the TAMC200 or its slot to be used in may occur!
Refer to the chapter "Component Height Violation on TAMC200-10R" for details.

3.3 Voltage Limits on IndustryPacks

The AMC.0 specification limits the voltages on AMC modules. These limits also apply to mount IndustryPacks.
Refer to the chapter "Voltage Limits on IndustryPack Modules" for details.

4 On Board Devices

4.1 Overview

The IndustryPack interface is implemented in an on board FPGA device, located on the local bus of a PCI9030 PCI target chip.

The PCI9030 PCI Target Chip is located on the TAMC200 embedded PCI bus.

A PEX8112 PCIe/PCI Bridge is used as the bridging device between the AMC PCIe interface and the on board PCI bus.

4.2 PEX8112 PCIe/PCI Bridge

The PEX8112 is a PCIe to PCI bridge. On the TAMC200 the PEX8112 is used in forward mode only.

4.2.1 PEX8112 Register Map

Register Group	PCI Space	Offset Address Range
PCI-Compatible Configuration (Type 1) Registers	PCI Express Configuration	0x00 - 0x3C
	Memory Mapped (BAR0)	
PCI-Compatible Extended Capability Registers for PCI Express Interface	PCI Express Configuration	0x40 - 0xFF
	Memory Mapped (BAR0)	
PCI Express Extended Capability Registers	PCI Express Configuration	0x100 - 0xFFF
	Memory Mapped (BAR0)	
Main Control Registers	Memory Mapped (BAR0)	0x1000 - 0x1FFF

Table 4-1 : PEX8112 Register Map

4.2.2 PCI Express Configuration Space Register Mapping

4.2.2.1 PCI-Compatible Configuration (Type 1) Registers

PCI CFG Register Address	31 24	23 16	15 8	7 0	Read after initialization write access
0x00	PCI Device ID		PCI Vendor ID		8112 10B5
0x04	PCI Status		PCI Command		0010 0000
0x08	PCI Class Code			PCI Device Revision ID	060400 AA
0x0C	PCI Built-In Self-Test (Not Supported)	PCI Header Type	Internal PCI Bus Latency Timer	PCI Cache Line Size	00 01 00 00
0x10	PCI Base Address 0				0000000C
0x14	PCI Base Address 1				00000000
0x18	Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	00 00 00 00
0x1C	Secondary Status		I/O Limit	I/O Base	0200 00 00
0x20	Memory Limit		Memory Base		0000 0000
0x24	Prefetchable Memory Limit		Prefetchable Memory Base		0000 0000
0x28	Prefetchable Memory Base Upper 32 Bits				00000000
0x2C	Prefetchable Memory Limit Upper 32 Bits				00000000
0x30	I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits		0000 0000
0x34	Reserved			PCI Capabilities Pointer	000000 40
0x38	PCI Base Address for Expansion ROM (Not Supported)				
0x3C	Bridge Control		Internal PCI Interrupt Wire	Internal PCI Interrupt Line	0000 01 00

Table 4-2 : PEX8112 PCI-Compatible Configuration (Type 1) Registers

4.2.2.2 PCI-Compatible Extended Capability Registers

PCI CFG Register Address	31 24	23 16	15 8	7 0	Read after initialization write access
0x40	Power Management Capabilities		Power Management Next Capability Pointer	Power Management Capability ID	CA02 5001
0x44	Power Management Data	Power Management Bridge Support	Power Management Control/Status		00 00 0000
0x48	Device-Specific Control				0000 0000
0x4C	Reserved				-
0x50	Message Singled Interrupts Control		Message Signaled Interrupts Next Capability Pointer	Message Signaled Interrupts Capability ID	0080 60 05
0x54	Message Signaled Interrupts Address				0000 0000
0x58	Message Signaled Interrupts Upper Address				0000 0000
0x5C	Reserved		Message Signaled Interrupts Data		0000 0000
0x60	PCI Express Capabilities		PCI Express Next Capability Pointer	PCI Express Capability ID	0071 00 10
0x64	Device Capabilities				0000 0000
0x68	PCI Express Device Status		PCI Express Device Control		0000 2000
0x6C	Link Capabilities				0000 4C11
0x70	Link Status		Link Control		1011 0000
0x74	Slot Capabilities				0000 0C80
0x78	Slot Status		Slot Control		0400 0000
0x7C	Reserved		Root Control		0000 0000
0x80	Root Status				0000 0000
0x84	Main Control Register Index				0000 0000
0x88	Main Control Register Data				0000 0000
0x8C - 0xFF	Reserved				-

Table 4-3 : PEX8112 PCI-Compatible Extended Capability Registers

4.2.3 Configuration EEPROM

After reset, the PEX8112 loads initial configuration register data from an on board configuration EEPROM. Only register settings differing from default values are stored in the EEPROM.

For detailed information please refer to the PEX8112 manual.

Modifications to default values are:

- Address Stepping is disabled (PCI Command Register)
- 66 MHz Capable Bit is cleared (I/O Limit & Secondary Status Register)
- Slot Clock Configuration is enabled (Link Status/Control Register)
- PCI Express Enable Bit is set (Device Initialization Register)

4.3 PCI9030 PCI Target Chip

The PCI9030 PCI Target Chip is the only PCI target device on the on board PCI bus (device number 0). The PCI9030 maps the IndustryPack Interface to the TAMC200 PCI bus (PCI memory space).

The IndustryPack interface and the IndustryPack interface control/status registers are mapped to local spaces of the PCI9030 PCI Target Chip (which in turn are mapped to the PCI memory space). Thus, the IndustryPack interface is mapped to the PCI memory space.

4.3.1 PCI9030 PCI Configuration Registers

Register Offset	PCI Configuration Register				Initial Configuration Setting
	31 … 24	23 … 16	15 … 8	7 … 0	
0x00	Device ID (PCI9030)		Vendor ID (PLX Technology)		9030 10B5
0x04	Status		Command		0280 0003
0x08	Class Code			Revision ID	0680 0000
0x0C	Not Supported	Header	Not Supported	Cache Line	0000 0000
0x10	PCI Base Address 0 (PCIBAR0) (PCI9030 Local Configuration Register Memory Mapped)				FFFF FF80 (128 Byte)
0x14	PCI Base Address 1 (PCIBAR1) (PCI9030 Local Configuration Register I/O Mapped) (disabled)				0000 0000
0x18	PCI Base Address 2 (PCIBAR2) (Local Space 0) **(IP Interface Control/Status Register)**				FFFF FF00(1) (256 Byte)
0x1C	PCI Base Address 3 (PCIBAR3) (Local Space 1) **(IP Interface I/O, ID, INT Space)**				FFFF FC00(1) (1 Kbyte)
0x20	PCI Base Address 4 (PCIBAR4) (Local Space 2) **(IP Interface Memory Space)**				FE00 0000(1) (32 Mbyte)
0x24	PCI Base Address 5 (PCIBAR5) (Local Space 3) **(IP Interface 8bit only Memory Space)**				FF00 0000(1) (16 Mbyte)
0x28	Not used				0000 0000
0x2C	Subsystem ID (TAMC200)		Subsystem Vendor ID (TEWS TECHNOLOGIES)		80C8 1498
0x30	PCI Expansion ROM Base Address				0000 0000
0x34	Reserved			Cap. Pointer	0000 0040
0x38	Reserved				0000 0000
0x3C	Not Supported	Not Supported	Interrupt Pin	Interrupt Line	0000 0100
0x40	PM Capabilities		PM NxtCap	PM CapID	4801 4801
0x44	PM Data	PM CSR EXT	PM CSR		0000 0000
0x48	Reserved	HS CSR	HS NxtCap	HS CapID	0000 4C06
0x4C	VPD Address		VPD NxtCap	VPD CapID	0000 0003
0x50	VPD Data				0000 0000

(1) Read back value after writing all 1's.

Table 4-4 : PCI9030 PCI Configuration Registers

4.3.2 Local Configuration Register

The PCI base address for the PCI9030 Local Configuration Registers (PCI Memory mapped) can be obtained from the PCIBAR0 register at offset 0x10 in the PCI9030 PCI configuration register space.

Register Offset	Local Configuration Register	Name	Setting
0x00	Local Space 0 Range	LAS0RR	0x0FFF_FF00
0x04	Local Space 1 Range	LAS1RR	0x0FFF_FC00
0x08	Local Space 2 Range	LAS2RR	0x0E00_0000
0x0C	Local Space 3 Range	LAS3RR	0x0F00_0000
0x10	Expansion ROM Range	EROMRR	0x0000_0000
0x14	Local Space 0 Remap	LAS0BA	0x0800_0001
0x18	Local Space 1 Remap	LAS1BA	0x0400_0001
0x1C	Local Space 2 Remap	LAS2BA	0x0000_0001
0x20	Local Space 3 Remap	LAS3BA	0x0200_0001
0x24	Expansion ROM Remap	EROMBA	0x0000_0000
0x28	Local Space 0 Descriptor	LAS0BRD	0xD441_60A0
0x2C	Local Space 1 Descriptor	LAS1BRD	0x1441_20A2
0x30	Local Space 2 Descriptor	LAS2BRD	0x1441_20A2
0x34	Local Space 3 Descriptor	LAS3BRD	0x1401_20A2
0x38	Expansion ROM Descriptor	EROMBRD	0x0000_0000
0x3C	Local Chip Select 0	CS0BASE	0x0800_0081
0x40	Local Chip Select 1	CS1BASE	0x0400_0201
0x44	Local Chip Select 2	CS2BASE	0x0100_0001
0x48	Local Chip Select 3	CS3BASE	0x0280_0001
0x4C	Serial EEPROM / Interrupt Control & Status	PROT_ AREA/ INTCSR	0x0030_0049
0x50	Miscellaneous	CNTRL	0x007A_5000
0x54	General Purpose I/O	GPIOC	0x0224_9252

Table 4-5 : PCI9030 Local Configuration Registers

Shown values are register values after serial EEPROM configuration.

4.3.3 Configuration EEPROM

After reset, the PCI9030 loads initial configuration register data from an on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x27 : PCI9030 PCI Configuration Register Values
- Address 0x28 to 0x87 : PCI9030 Local Configuration Register Values
- Address 0x88 to 0xFF : Reserved

See the PCI9030 Manual for more information.

EEPROM Address	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x9030	0x10B5	0x0280	0x0000	0x0680	0x0000	0x80C8	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x4801	0x0000	0x0000
0x20	0x0000	0x4C06	0x0000	0x0003	0x0FFF	0xFF00	0x0FFF	0xFC00
0x30	0x0E00	0x0000	0x0F00	0x0000	0x0000	0x0000	0x0800	0x0001
0x40	0x0400	0x0001	0x0000	0x0001	0x0200	0x0001	0x0000	0x0000
0x50	0xD441	0x60A0	0x1441	0x20A2	0x1441	0x20A2	0x1401	0x20A2
0x60	0x0000	0x0000	0x0800	0x0081	0x0400	0x0201	0x0100	0x0001
0x70	0x0280	0x0001	0x0030	0x0049	0x007A	0x5000	0x0224	0x9252
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 4-6 : PCI9030 Configuration EEPROM Content

4.4 FPGA

An FPGA resides on the PCI9030 local bus.

The FPGA implements the IndustryPack Interface Control/Status Registers and maps the IndustryPack slots to the PCI9030 local bus.

The FPGA configures from a serial Flash after power-up. An on board SMD LED indicates successful FPGA configuration.

5 IP Interface Address Map

The IP Interface and the IP Interface Control/Status registers are mapped to the on board PCI bus via the local spaces of the on board PCI9030 PCI Target Chip.

5.1 PCI9030 PCI Base Address Configuration

The PCI9030 local spaces are used to access the IP interface and the IP Interface Control/Status registers.

The PCI base address for each local space is obtained from the PCI9030 PCI configuration register space.

PCI9030 PCI BAR	PCI9030 Local Space	Size (Byte)	Port Width (Bit)	Endian Mode	PCI Space	IP Interface Space
2	0	256	16	Little	MEM	IP Interface Control/Status Register
3	1	1 K	16	Little	MEM	IP A-C ID, INT, IO Space (8/16 bit)
4	2	32 M	16	Little	MEM	IP A-C MEM Space (8/16 bit)
5	3	16 M	8	Little	MEM	IP A-C MEM Space (8 bit only port)

Table 5-1 : PCI9030 PCI Base Address Configuration

Note: The PCI9030 will convert 32 bit transfer-size access to the actual port width. E.g. an aligned 32 bit write to a 16 bit port is automatically splitted into two 16 bit writes.

5.1.1 IP Interface Register Map

The PCI9030 BAR 2 space is used for the IP interface control/status registers.

The following control/status registers are implemented:

PCI Base Address: PCI9030 PCI Base Address 2 (Offset 0x18 in the PCI9030 PCI configuration register space).

Offset (Base = PCI Base Address 2)	Size (Byte)	Register
0x00	2	REVISION ID
0x02	2	IP A CONTROL
0x04	2	IP B CONTROL
0x06	2	IP C CONTROL
0x08	2	Reserved
0x0A	2	IP RESET
0x0C	2	IP STATUS
0x0E	2	Reserved
0x10 - 0xFF	240	Reserved

Table 5-2 : IP Interface Register Map

5.1.1.1 Revision ID Register (Offset 0x00)

The Revision ID Register shows the revision of the on board IP FPGA logic.

Bit	Name	Description
15 (MSB)	-	Read : Undefined Write : No Effect
14		
13		
12		
11		
10		
9		
8		
7	REV_ID	Read: FPGA Logic Revision ID Write : No Effect
6		
5		
4		
3		
2		
1		
0 (LSB)		

Table 5-3 : IP Interface Revision ID Register

5.1.1.2 IP Control Registers (Offsets 0x02, 0x04, 0x06)

The IP Control Registers are used to control IP interrupts, recover time and clock rate on the IP interface.

There is one IP Control Register for each IP Slot (A-C).

Bit	Name	Description
15 (MSB)	-	Read : Undefined Write : No Effect. Should be written with 0's
14		
13		
12		
11		
10		
9		
8	SEL_MODE	0 : Single IP Select Cycle 1 : Extended IP Select Cycle IP Select is held active until the first IP Acknowledge Cycle is detected. May be required by some IP modules.
7	INT1_EN	0 : IP Interrupt 1 Disabled 1 : IP Interrupt 1 Enabled
6	INT0_EN	0 : IP Interrupt 0 Disabled 1 : IP Interrupt 0 Enabled
5	INT1_SENSE	0 : IP Interrupt 1 Level Sensitive 1 : IP Interrupt 1 Edge Sensitive
4	INT0_SENSE	0 : IP Interrupt 0 Level Sensitive 1 : IP Interrupt 0 Edge Sensitive
3	ERR_INT_EN	0 : IP Error Interrupt Disabled 1 : IP Error Interrupt Enabled
2	TIME_INT_EN	0 : IP Timeout Interrupt Disabled 1 : IP Timeout Interrupt Enabled
1	RECOVER	0 : IP Recover Time Disabled 1 : IP Recover Time Enabled
0 (LSB)	CLKRATE	0 : IP Clock Rate 8 MHz 1 : IP Clock Rate 32 MHz

Table 5-4 : IP Interface Control Registers

After reset, all bits in the IP Control Registers are cleared.

If IP recover time is enabled for an IP slot, an IP cycle for this slot will not begin until the IP recover time is expired. The IP recover time is app. 1µs.

5.1.1.3 IP Reset Register (Offset 0x0A)

The IP Reset Register is used to assert the IP RESET# signal and to detect when the IP reset phase is done.

Bit	Name	Description
15 (MSB)	-	Read : Undefined Write : No Effect. Should be written with 0's
14		
13		
12		
11		
10		
9		
8		
7		
6		
5		
4		
3		
2		
1		
0 (LSB)	IP_RESET	Read : 0 : IP RESET# Signal is De-asserted 1 : IP RESET# Signal is Asserted Write : 0 : No Effect 1 : Assert IP RESET# Signal (Automatic Negation)

Table 5-5 : IP Interface Reset Register

The IP RESET# signal is also asserted during payload reset.

5.1.1.4 IP Status Register (Offset 0x0C)

The IP Status Register is used to read IP timeout, error and interrupt status for the IP slots.

The IP timeout time is app. 8µs.

An IP timeout occurs if the IP module fails to generate the IP ACK# signal within the IP timeout time. An IP timeout is not reported to the PCI9030 or the PCI Master, but in the Status Register. For timeout reads all F's are returned as read data.

Bit	Name	Description
15 (MSB)	-	Reserved. Undefined for reads.
14	TIME_C	Read : 0 : No Timeout on IP_C 1 : IP_C Timeout has occurred Write : 0 : No Effect 1 : Clear IP_C Timeout Status
13	TIME_B	Read : 0 : No Timeout on IP_B 1 : IP_B Timeout has occurred Write : 0 : No Effect 1 : Clear IP_B Timeout Status
12	TIME_A	Read : 0 : No Timeout on IP_A 1 : IP_A Timeout has occurred Write : 0 : No Effect 1 : Clear IP_A Timeout Status
11	-	Reserved. Undefined for reads.
10	ERR_C	Read : 0 : No Error on IP_C 1 : IP_C ERROR# Signal Asserted Write : No Effect
9	ERR_B	Read : 0 : No Error on IP_B 1 : IP_B ERROR# Signal Asserted Write : No Effect
8	ERR_A	Read : 0 : No Error on IP_A 1 : IP_A ERROR# Signal Asserted Write : No Effect
7	-	Reserved. Undefined for reads.
6	-	Reserved.

Bit	Name	Description
		Undefined for reads.
5	INT1_C	Read : 0 : No Interrupt 1 Request on IP_C 1 : Active IP_C Interrupt 1 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_C Interrupt 1 Status
4	INT0_C	Read : 0 : No Interrupt 0 Request on IP_C 1 : Active IP_C Interrupt 0 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_C Interrupt 0 Status
3	INT1_B	Read : 0 : No IP_B Interrupt 1 Request 1 : Active IP_B Interrupt 1 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_B Interrupt 1 Status
2	INT0_B	Read : 0 : No Interrupt 0 Request on IP_B 1 : Active IP_B Interrupt 0 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_B Interrupt 0 Status
1	INT1_A	Read : 0 : No Interrupt 1 Request on IP_A 1 : Active IP_A Interrupt 1 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_A Interrupt 1 Status
0 (LSB)	INT0_A	Read : 0 : No Interrupt 0 Request on IP_A 1 : Active IP_A Interrupt 0 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_A Interrupt 0 Status

Table 5-6 : IP Interface Status Register

5.1.2 IP Interface I/O, ID, INT Space Address Map

The PCI9030 BAR 3 space is used for the IP A-C I/O, ID and INT space.

PCI Base Address: PCI9030 PCI Base Address 3 (Offset 0x1C in the PCI9030 PCI configuration register space).

Offset (Base = PCI Base Address 3)		Size (Byte)	IP Slot	IP Space
Start	End			
0x0000_0000	0x0000_007F	128	A	I/O
0x0000_0080	0x0000_00BF	64	A	ID
0x0000_00C0	0x0000_00FF	64	A	INT
0x0000_0100	0x0000_017F	128	B	I/O
0x0000_0180	0x0000_01BF	64	B	ID
0x0000_01C0	0x0000_01FF	64	B	INT
0x0000_0200	0x0000_027F	128	C	I/O
0x0000_0280	0x0000_02BF	64	C	ID
0x0000_02C0	0x0000_02FF	64	C	INT
0x0000_0300	0x0000_03FF	256	Reserved	

Table 5-7 : IP I/O, ID, INT Space Address Map

The TAMC200 will perform write cycles to the IP ID space.

Any access to the IP INT space will assert the IP INTSEL# signal on the selected IP slot. The TAMC200 will perform write cycles to the IP INT space.

The user should perform IP INT space read cycles on the desired IP slot to generate an IP INTSEL# cycle and read the interrupt vector from the IP module. For this read cycle the address must reflect if the IP INTSEL# cycle is for IP INT0# (additional offset 0x0) or for IP INT1# (additional offset 0x2).

5.1.3 IP Interface Memory Space Address Map

The PCI9030 BAR 4 space is used for the IP A-C Memory space (8/16 bit).

PCI Base Address: PCI9030 PCI Base Address 4 (Offset 0x20 in the PCI9030 PCI configuration register space).

Offset (Base = PCI Base Address 4)		Size (Byte)	IP Slot	IP Space
Start	End			
0x0000_0000	0x007F_FFFF	8 M	A	MEM (16 bit)
0x0080_0000	0x00FF_FFFF	8 M	B	MEM (16 bit)
0x0100_0000	0x017F_FFFF	8 M	C	MEM (16 bit)
0x0180_0000	0x01FF_FFFF	8 M	Reserved	

Table 5-8 : IP Memory Space Address Map

5.1.4 IP Interface 8 bit only Memory Space Address Map

The PCI9030 BAR 5 space is used for the IP A-C Memory space for 8 bit only configurations.

PCI Base Address: PCI9030 PCI Base Address 5 (Offset 0x24 in the PCI9030 PCI configuration register space).

Offset (Base = PCI Base Address 5)		Size (Byte)	IP Slot	Description
Start	End			
0x0000_0000	0x003F_FFFF	4 M	A	MEM Space (8 bit)
0x0040_0000	0x007F_FFFF	4 M	B	MEM Space (8 bit)
0x0080_0000	0x00BF_FFFF	4 M	C	MEM Space (8 bit)
0x00C0_0000	0x00FF_FFFF	4 M	Reserved	

Table 5-9 : IP 8 bit only Memory Space Address Map

The 8 bit IP Memory space should be used for memory space linear byte addressing of IP modules that use IP data lines D[7:0] only.

6 Interrupts

6.1 Interrupt Sources

The TAMC200 provides the following main interrupt sources:

- IP_A_INT#[1:0]
- IP_B_INT#[1:0]
- IP_C_INT#[1:0]

All the IP interrupts are low active and may be set to level or edge sensitive by the IP Control registers.

Note that there are additional interrupt sources, since both the PCI9030 and the PEX8112 provide the capability of Software controlled or internally generated interrupts. None of these interrupts is used for the main TAMC200 functionality.

6.2 Interrupt Mapping

The IP Interface Address Map provides an interrupt status register as well as register bits for interrupt enable control.

If any of the interrupt bits is set in the IP status register and the corresponding interrupt enable bit is set in the IP control register, the PCI9030 LINT1# line on the PCI9030 local bus is asserted.

Upon LINT1# assertion, the PCI9030 asserts the INTA# line on the PCI bus (if enabled in the PCI9030 Interrupt Control/Status register).

The INTA# line of the TMC200 local PCI bus connects to the INTA# pin of the PEX8112.

On the PEX8112, in Forward Bridge mode, INTA# is an input from the PCI bus. The PEX8112 maps INTA# activity into Assert_INTx or Deassert_INTx messages on the PCI Express interface.

6.3 Interrupt Handling

Upon receiving a PCI Express Assert_INTA message, Software should check the PCI9030 Interrupt Control/Status register. Interrupts from the IP interface will have the LINTi1 Status bit set. The PCI9030 local bus interrupts are set to be level sensitive, so no need for clearing here.

Upon detecting IP interrupts, Software should check the IP Status register to determine which IP interrupts are active.

For edge sensitive IP interrupts, the interrupt is cleared by writing a 1 to the corresponding bit in the IP Status register. For level sensitive IP interrupts, interrupt clearing is scope of the IP module used.

7 Module Management

7.1 Front Panel LEDs (MMC controlled)

For a quick visual inspection the TAMC200 provides several LEDs in the front panel and also some on board LEDs. See I/O Description section for non-MMC-controlled LEDs.

LED	Color	State	Description
HS	Blue	Off	No Power or module is powered
		Short Blink	Hot-Swap negotiation (extraction)
		Long Blink	Hot-Swap negotiation (insertion)
		On	Module is ready to be powered or module is ready to be unpowered
FAIL	Red	Off	No Failure
		On	Failure or out of service status
ACT	Green	Off	Board is not powered up
		On	Board is powered and OK
		On (Off Flash)	PCI bus activity

Table 7-1 : Front Panel LEDs (MMC controlled)

7.2 Temperature and Voltage Sensors

Sensor Number	Signal Type	Signal Monitored
0	Event	Hot-swap switch
1	Temperature	LM75 #1
2	Temperature	LM75 #2
3	Voltage	+12V (PWR)
4	Voltage	+1.5V
5	Voltage	+12V (IP)
6	Voltage	-12V (IP)

Table 7-2 : Temperature and Voltage Sensors

7.3 FRU Data Multi-Records

7.3.1 Connectivity Record

The TAMC200 FRU data provides a connectivity record with the following settings.

Single x1 2.5 Gbps PCI-Express Link on AMC Port 4.

The PCI-Express Interface works with SSC and non SSC PCI-Express Reference Clocks.

7.3.2 Module Current Requirement Record

The TAMC200 FRU data provides the following Module Current Requirement record setting.

FRU Data / Module Current Requirement Record / Current Draw value = 4A.

7.3.3 Clock Configuration Record

The TAMC200 FRU data provides a clock configuration record for FCLKA.

FCLKA: Activated by Carrier, Receiver (no PLL), PCI Express G1

8 Installation

8.1 AMC Module Insertion & Hot-Swap

8.1.1 Insertion

Handle	Blue LED	Description
Open (Full extracted)	OFF	Insert Module into slot
Open (Full extracted)	ON	Module is ready to attempt activation
Closed (Pushed all way in)	Long Blink	Hot-Swap Negotiation
Closed (Pushed all way in)	OFF	Module is ready & powered

Table 8-1 : AMC Module Insertion

When the blue LED does not go off but remains in the “ON” state, the module FRU (Field Replaceable Unit) information is invalid or the system cannot provide the requested & required power.

8.1.2 Extraction

Handle	Blue LED	Description
Pulled out 1/2	OFF	Request Hot-Swap
Pulled out 1/2	Short Blink	Hot-Swap Negotiation
Pulled out 1/2	ON	Module is ready to be extracted
Open (Full extracted)	ON	Extract Module from slot

Table 8-2 : AMC Module Extraction

8.2 Installation of IndustryPacks

Before installing an IndustryPack, be sure that the power supply for the TAMC200 is turned off.

The component is sensitive to Electrostatic Discharge (ESD). Use an anti-static mat connected to a wristband when handling or installing the components.

Installing IndustryPacks on the TAMC200 is done by simply snapping them into the IP slot. The connectors are keyed, so the IndustryPack can only be installed correctly. After an IP has been installed it can be fastened to the carrier board by screws. This is normally necessary only in high vibration or shock environments. Screws and spacers are required to fix a single IP on the TAMC200. They can be ordered from TEWS TECHNOLOGIES (Part number: TIPxxx-HK).

8.3 Component Height Violation on TAMC200-10R

The TAMC200 mid-size option (TAMC200-10R) will violate the AMC.0 R2.0 component height limits on component side 1 envelopes 1 and 2 when IndustryPack modules are installed.

With a standard IndustryPack module of 1.6mm PCB thickness, the height limit of envelope 1 is violated by 0.38 mm and the height limit of envelope 2 is violated by 1.74 mm. The figure below shows the violation of the AMC component envelopes in red.

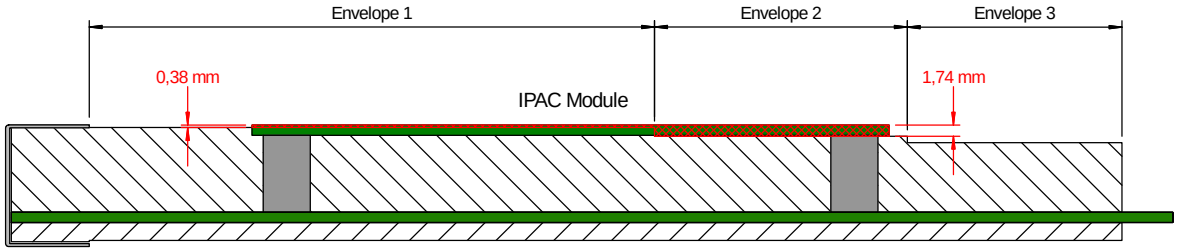

Figure 8-1 : Component Height Violation

The TAMC200-10R is intended for the use in µTCA systems where the adjacent AMC module provides enough spacing (no components on the adjacent AMC modules back side) for the protruding IndustryPack module. This allows improving the density of the µTCA system.

If any of the mounted IndustryPack modules has devices assembled on its back side or if it can not be guaranteed that the available spacing is sufficient, it is strongly recommended to use the full-height TAMC200-11R. It is within the responsibility of the user to carefully check if the mid-size module with its component height violation can be used in his system. Otherwise damage of the TAMC200 or its slot to be used in may occur!

8.4 Voltage Limits for IndustryPack Modules

The AMC.0 specification defines the following limits for voltages on AMC modules:

	DC voltage	AC voltage
Positive	+27V	+27V peak
Negative	-15V	-15V peak

Table 8-3 : IP Voltage Limits

With IndustryPack modules exceeding these limits, additional insulation to adjacent modules or carrier boards may be required.

8.5 IP Power Supply Filters

The TAMC200 provides RF filtering and decoupling capacitors on all IP power lines.

There are 3 power supply filters (Murata Type NFM61R00T361) for each IP slot. One for the +12V supply pin, one for the -12V supply pin and one for the two +5V supply pins.

8.6 IP Power Supply Fuses

There is a resettable fuse for the +5V supply at each IP slot.

Type: Bourns MF-MSMF200 (R1 max 0.080 Ohm)

IP 5V Fuse Operating Current Rating I_hold (Ampere) @ TA								
-40°C	-20°C	0°C	23°C	40°C	50°C	60°C	70°C	85°C
3.08	2.71	2.35	2.00	1.80	1.60	1.50	1.40	1.25

Table 8-4 : IP +5V Fuse Operating Current Rating

There is a resettable fuse for the +12V supply and a PolyFuse for the -12V supply at each IP slot.

Type: Bourns MF-NSMF020 (R1 max 2.60 Ohm)

IP +12V/-12V Fuse Operating Current Rating I_hold (Ampere) @ TA								
-40°C	-20°C	0°C	23°C	40°C	50°C	60°C	70°C	85°C
0.30	0.27	0.24	0.20	0.18	0.16	0.14	0.12	0.11

Table 8-5 : IP +12V/-12V Fuse Operating Current Rating

8.7 IP Power Supply Rating

IP Power Supply	Max. Current Rating See also Fuse section for temperature table
+5V	**max 2A per IP slot** (TA <= 23°C, less for higher temperatures)
+12V	**max 500mA total, max 200mA for an IP slot @ 23°C** (e.g. the IP modules in slots A & B may use 200mA each on +12V while the IP module in slot C is using 100mA on +12V)
-12V	**max 300mA total, max 200mA for an IP slot @ 23°C** (e.g. the IP module in slot A may use 200mA on -12V, while the IP module in slot B uses 100mA on -12V and the IP module in slot C does not use the -12V)

Table 8-6 : IP Power Supply Rating

8.8 IP Logic Interface

The IP logic interface signals driven by the TAMC200 IP carrier have LVTTL signal levels (3.3V high level), except IP_RESET#, which is a 5V level signal.

IP modules may drive LVTTL, TTL or 5V CMOS signal levels.

8.9 IP I/O Interface

All pins of the IP slot I/O connectors are available at the front plate.

The TAMC200 IP I/O lines have a max current rating of 0.3A (max rating of the VHDCI connector).

9 I/O Description

9.1 I/O Overview

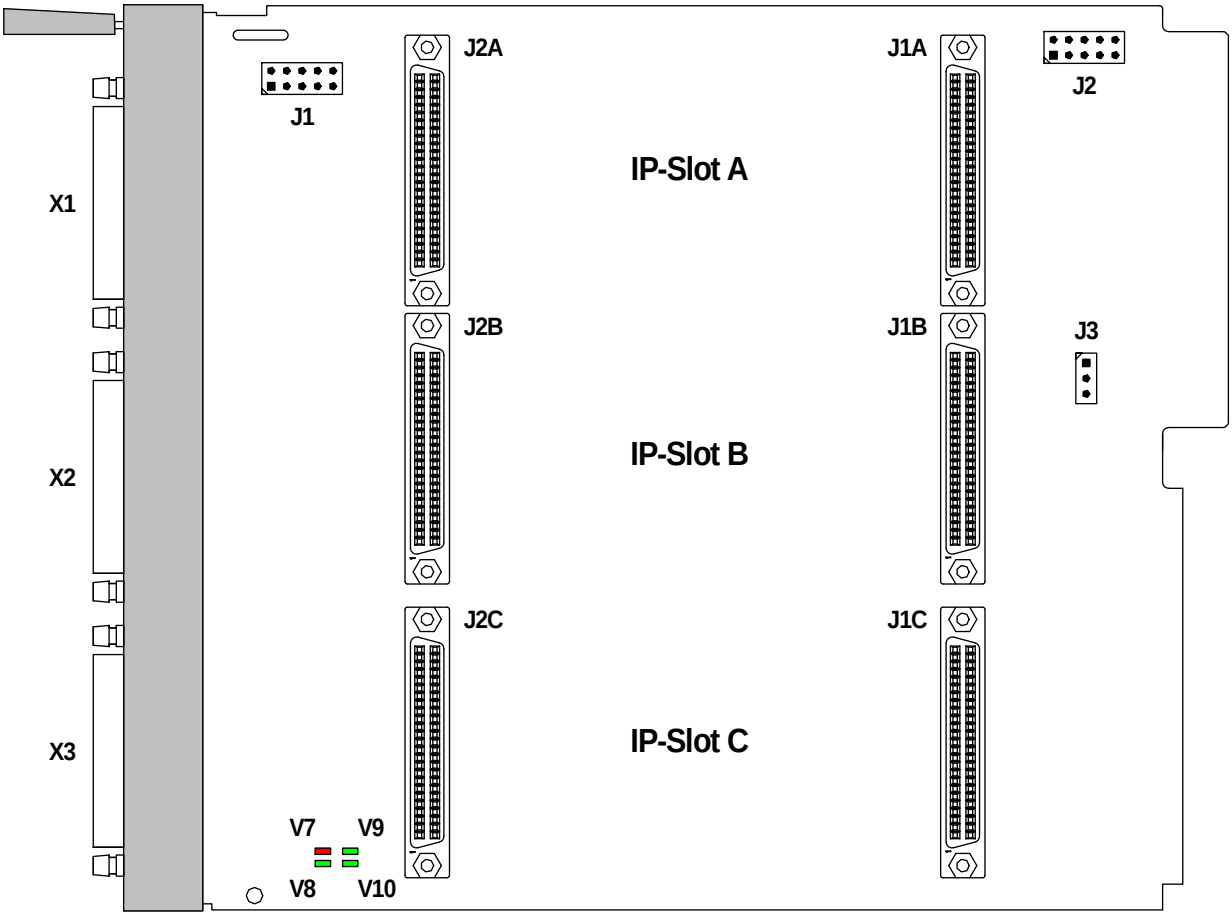

Figure 9-1 : Header, Connector, LED Location

ID	Description
J1	Factory Only (Do not use)
J2	Factory Only (Do not use)
J3	IP Strobe Header
J1A	IP Slot A Logic Interface Connector
J2A	IP Slot A I/O Interface Connector
J1B	IP Slot B Logic Interface Connector
J2B	IP Slot B I/O Interface Connector
J1C	IP Slot C Logic Interface Connector
J2C	IP Slot C I/O Interface Connector
V7	LINK_DOWN LED (red)
V8	FPGA_DONE LED (green)
V9	5V_OK LED (green)
V10	3V3_OK LED (green)
X1	IP A I/O Connector
X2	IP B I/O Connector
X3	IP C I/O Connector

Table 9-1 : Header, Connector, LED Description

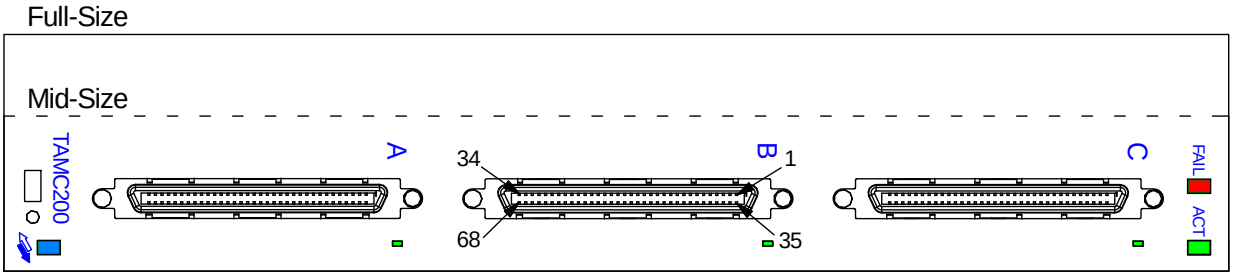

Figure 9-2 : Front Panel Overview

9.2 LED Indicators

See Module Management section for MMC controlled LEDs.

9.2.1 Front Panel LEDs (IP Interface Controlled)

LED	Color	State	Description
A	Green	On (flash)	IP Slot A IP Access Acknowledge
		Off	IP Slot A No IP Access or IP Slot A 5V Power Supply invalid
B	Green	On (flash)	IP Slot B IP Access Acknowledge
		Off	IP Slot B No IP Access or IP Slot B 5V Power Supply invalid
C	Green	On (flash)	IP Slot C IP Access Acknowledge
		Off	IP Slot C No IP Access or IP Slot C 5V Power Supply invalid

Table 9-2 : Front Panel LEDs (IP Interface Controlled)

9.2.2 On Board LEDs

LED	Color	State	Description
Link Down	Red	Off	PCIe link is up
		On	PCIe link is down
FPGA Done	Green	Off	FPGA is not configured
		On	FPGA is configured
+5V Power Good	Green	Off	+5V Power Supply is not OK
		On	+5V Power Supply is OK
+3.3V Power Good	Green	Off	+3.3V Power Supply is not OK
		On	+3.3V Power Supply is OK

Table 9-3 : On Board LEDs

9.3 Pin Assignments

9.3.1 IP A J1 Connector

Pin-Count	50
Connector Type	AMPLIMITE 0.50 Series
Source & Order Info	5173280-3 (Tyco)
Location	On board

Pin Assignment		
Pin	**Description**	**Note**
1	GND	
2	IP_A_CLK	
3	IP_RESET#	Common to all IP slots
4	IP_AC_D00	
5	IP_AC_D01	
6	IP_AC_D02	
7	IP_AC_D03	
8	IP_AC_D04	
9	IP_AC_D05	
10	IP_AC_D06	
11	IP_AC_D07	
12	IP_AC_D08	
13	IP_AC_D09	
14	IP_AC_D10	
15	IP_AC_D11	
16	IP_AC_D12	
17	IP_AC_D13	
18	IP_AC_D14	
19	IP_AC_D15	
20	IP_A_BS0#	
21	IP_A_BS1#	
22	IP_A_-12V	Fused for 200mA @ 23°C
23	IP_A_+12V	Fused for 200mA @ 23°C
24	IP_A_+5V	Fused for 2A @ 23°C (common fuse for pins 24 & 27)
25	GND	
26	GND	
27	IP_A_+5V	Fused for 2A @ 23°C (common fuse for pins 24 & 27)
28	IP_WRITE#	Common to all IP slots

29	IP_A_IDSEL#	
30	(IP_A_DMAREQ0#)	Not supported, Pull-up to 5V
31	IP_A_MEMSEL#	
32	(IP_A_DMAREQ1#)	Not supported, Pull-up to 5V
33	IP_A_INTSEL#	
34	(IP_A_DMAACK#)	Not supported, Pull-up to 5V
35	IP_A_IOSEL#	
36	IP_A_RESERVED0	Pull-up to 5V
37	IP_A1	Common to all IP slots
38	(IP_A_DMAEND#)	Not supported, Pull-up to 5V
39	IP_A2	Common to all IP slots
40	IP_A_ERROR#	Pull-up to 5V
41	IP_A3	Common to all IP slots
42	IP_A_INTREQ0#	Pull-up to 5V
43	IP_A4	Common to all IP slots
44	IP_A_INTREQ1#	Pull-up to 5V
45	IP_A5	Common to all IP slots
46	IP_A_STROBE#	On board header
47	IP_A6	Common to all IP slots
48	IP_A_ACK#	Pull-up to 5V
49	IP_A_RESERVED1	Pull-up to 5V
50	GND	

Table 9-4 : IP Slot A J1 Connector

9.3.2 IP B J1 Connector

Pin-Count	50	
Connector Type	AMPLIMITE 0.50 Series	
Source & Order Info	5173280-3 (Tyco)	
Location	On board	
Pin Assignment		
Pin	**Description**	**Note**
1	GND	
2	IP_B_CLK	
3	IP_RESET#	Common to all IP slots
4	IP_B_D00	
5	IP_ B_D01	
6	IP_B_D02	

7	IP_B_D03	
8	IP_B_D04	
9	IP_B_D05	
10	IP_B_D06	
11	IP_B_D07	
12	IP_B_D08	
13	IP_B_D09	
14	IP_B_D10	
15	IP_B_D11	
16	IP_B_D12	
17	IP_B_D13	
18	IP_B_D14	
19	IP_B_D15	
20	IP_B_BS0#	
21	IP_B_BS1#	
22	IP_B_-12V	Fused for 200mA @ 23°C
23	IP_B_+12V	Fused for 200mA @ 23°C
24	IP_B_+5V	Fused for 2A @ 23°C (common fuse for pins 24 & 27)
25	GND	
26	GND	
27	IP_B_+5V	Fused for 2A @ 23°C (common fuse for pins 24 & 27)
28	IP_WRITE#	Common to all IP slots
29	IP_B_IDSEL#	
30	(IP_B_DMAREQ0#)	Not supported, Pull-up to 5V
31	IP_B_MEMSEL#	
32	(IP_B_DMAREQ1#)	Not supported, Pull-up to 5V
33	IP_B_INTSEL#	
34	(IP_B_DMAACK#)	Not supported, Pull-up to 5V
35	IP_B_IOSEL#	
36	IP_B_RESERVED0	Pull-up to 5V
37	IP_A1	Common to all IP slots
38	(IP_B_DMAEND#)	Not supported, Pull-up to 5V
39	IP_A2	Common to all IP slots
40	IP_B_ERROR#	Pull-up to 5V
41	IP_A3	Common to all IP slots

42	IP_B_INTREQ0#	Pull-up to 5V
43	IP_A4	Common to all IP slots
44	IP_B_INTREQ1#	Pull-up to 5V
45	IP_A5	Common to all IP slots
46	IP_B_STROBE#	On board header
47	IP_A6	Common to all IP slots
48	IP_B_ACK#	Pull-up to 5V
49	IP_B_RESERVED1	Pull-up to 5V
50	GND	

Table 9-5 : IP Slot B J1 Connector

9.3.3 IP C J1 Connector

Pin-Count	50	
Connector Type	AMPLIMITE 0.50 Series	
Source & Order Info	5173280-3 (Tyco)	
Location	On board	
Pin Assignment		
Pin	**Description**	**Note**
1	GND	
2	IP_C_CLK	
3	IP_RESET#	Common to all IP slots
4	IP_AC_D00	
5	IP_AC_D01	
6	IP_AC_D02	
7	IP_AC_D03	
8	IP_AC_D04	
9	IP_AC_D05	
10	IP_AC_D06	
11	IP_AC_D07	
12	IP_AC_D08	
13	IP_AC_D09	
14	IP_AC_D10	
15	IP_AC_D11	
16	IP_AC_D12	
17	IP_AC_D13	
18	IP_AC_D14	
19	IP_AC_D15	
20	IP_C_BS0#	
21	IP_C_BS1#	
22	IP_C_-12V	Fused for 200mA @ 23°C

23	IP_C_+12V	Fused for 200mA @ 23°C
24	IP_C_+5V	Fused for 2A @ 23°C (common fuse for pins 24 & 27)
25	GND	
26	GND	
27	IP_C_+5V	Fused for 2A @ 23°C (common fuse for pins 24 & 27)
28	IP_WRITE#	Common to all IP slots
29	IP_C_IDSEL#	
30	(IP_C_DMAREQ0#)	Not supported, Pull-up to 5V
31	IP_C_MEMSEL#	
32	(IP_C_DMAREQ1#)	Not supported, Pull-up to 5V
33	IP_C_INTSEL#	
34	(IP_C_DMAACK#)	Not supported, Pull-up to 5V
35	IP_C_IOSEL#	
36	IP_C_RESERVED0	Pull-up to 5V
37	IP_A1	Common to all IP slots
38	(IP_C_DMAEND#)	Not supported, Pull-up to 5V
39	IP_A2	Common to all IP slots
40	IP_C_ERROR#	Pull-up to 5V
41	IP_A3	Common to all IP slots
42	IP_C_INTREQ0#	Pull-up to 5V
43	IP_A4	Common to all IP slots
44	IP_C_INTREQ1#	Pull-up to 5V
45	IP_A5	Common to all IP slots
46	IP_C_STROBE#	On board header
47	IP_A6	Common to all IP slots
48	IP_C_ACK#	Pull-up to 5V
49	IP_C_RESERVED1	Pull-up to 5V
50	GND	

Table 9-6 : IP Slot C J1 Connector

9.3.4 IP x J2 Connector (x = A, B, C)

Pin-Count	50
Connector Type	AMPLIMITE 0.50 Series
Source & Order Info	5173280-3 (Tyco)

Location	On board	
Pin Assignment		
Pin	**Description**	**Note**
1	IP_x_IO_01	
2	IP_x_IO_02	
3	IP_x_IO_03	
4	IP_x_IO_04	
5	IP_x_IO_05	
6	IP_x_IO_06	
7	IP_x_IO_07	
8	IP_x_IO_08	
9	IP_x_IO_09	
10	IP_x_IO_10	
11	IP_x_IO_11	
12	IP_x_IO_12	
13	IP_x_IO_13	
14	IP_x_IO_14	
15	IP_x_IO_15	
16	IP_x_IO_16	
17	IP_x_IO_17	
18	IP_x_IO_18	
19	IP_x_IO_19	
20	IP_x_IO_20	
21	IP_x_IO_21	
22	IP_x_IO_22	
23	IP_x_IO_23	
24	IP_x_IO_24	
25	IP_x_IO_25	
26	IP_x_IO_26	
27	IP_x_IO_27	
28	IP_x_IO_28	
29	IP_x_IO_29	
30	IP_x_IO_30	
31	IP_x_IO_31	
32	IP_x_IO_32	
33	IP_x_IO_33	
34	IP_x_IO_34	
35	IP_x_IO_35	
36	IP_x_IO_36	
37	IP_x_IO_37	
38	IP_x_IO_38	

39	IP_x_IO_39	
40	IP_x_IO_40	
41	IP_x_IO_41	
42	IP_x_IO_42	
43	IP_x_IO_43	
44	IP_x_IO_44	
45	IP_x_IO_45	
46	IP_x_IO_46	
47	IP_x_IO_47	
48	IP_x_IO_48	
49	IP_x_IO_49	
50	IP_x_IO_50	

Table 9-7 : IP J2 I/O Connectors (on board)

9.3.5 IP x I/O Connector (x = A, B, C)

Pin-Count	68	
Connector Type	VHDCI Female 68pos. 0.8mm spacing	
Source & Order Info	HDRA-EC68LFDT-SL+ (Honda)	
Location	Front plate	
Pin Assignment		
Pin	**Description**	**Note**
1	IP_x_IO_01	0.3A max
2	IP_x_IO_02	0.3A max
3	IP_x_IO_03	0.3A max
4	IP_x_IO_04	0.3A max
5	IP_x_IO_05	0.3A max
6	IP_x_IO_06	0.3A max
7	IP_x_IO_07	0.3A max
8	IP_x_IO_08	0.3A max
9	IP_x_IO_09	0.3A max
10	IP_x_IO_10	0.3A max
11	IP_x_IO_11	0.3A max
12	IP_x_IO_12	0.3A max
13	IP_x_IO_13	0.3A max
14	IP_x_IO_14	0.3A max
15	IP_x_IO_15	0.3A max
16	IP_x_IO_16	0.3A max
17	IP_x_IO_17	0.3A max
18	IP_x_IO_18	0.3A max
19	IP_x_IO_19	0.3A max

20	IP_x_IO_20	0.3A max
21	IP_x_IO_21	0.3A max
22	IP_x_IO_22	0.3A max
23	IP_x_IO_23	0.3A max
24	IP_x_IO_24	0.3A max
25	IP_x_IO_25	0.3A max
26	IP_x_IO_26	0.3A max
27	IP_x_IO_27	0.3A max
28	IP_x_IO_28	0.3A max
29	IP_x_IO_29	0.3A max
30	IP_x_IO_30	0.3A max
31	IP_x_IO_31	0.3A max
32	IP_x_IO_32	0.3A max
33	IP_x_IO_33	0.3A max
34	IP_x_IO_34	0.3A max
35	IP_x_IO_35	0.3A max
36	IP_x_IO_36	0.3A max
37	IP_x_IO_37	0.3A max
38	IP_x_IO_38	0.3A max
39	IP_x_IO_39	0.3A max
40	IP_x_IO_40	0.3A max
41	IP_x_IO_41	0.3A max
42	IP_x_IO_42	0.3A max
43	IP_x_IO_43	0.3A max
44	IP_x_IO_44	0.3A max
45	IP_x_IO_45	0.3A max
46	IP_x_IO_46	0.3A max
47	IP_x_IO_47	0.3A max
48	IP_x_IO_48	0.3A max
49	IP_x_IO_49	0.3A max
50	IP_x_IO_50	0.3A max
51 - 68	NC	

Table 9-8 : IP I/O Connectors (Front Panel)

9.3.6 IP Strobe Signal Header

The Strobe Header may be used to connect the Strobe signals of mounted IP modules.

Pin-Count	3
Connector Type	Std. 1-row 3 Pin Header
Source & Order Info	-
Location	On board

Pin Assignment		
Pin	**Description**	**Note**
1	IP_A_STROBE#	Square pad
2	IP_B_STROBE#	
3	IP_C_STROBE#	

Table 9-9 : IP Strobe Signal Header